

MCIMX6UL-BB

Schematics DevBoard

Table of Content


Page 1	Cover
Page 2	Block Diagram
Page 3	PWR TREE
Page 4	LCD
Page 5	HDMI
Page 6	USB
Page 7	CAN
Page 8	Sensor
Page 9	Codec
Page 10	Ethernet x1
Page 11	Ethernet x2
Page 12	SD/BT
Page 13	Camera
Page 14	DBG/JTAG
Page 15	SYS PWR
Page 16	SODIMM BB
Page 17	NOTE
Page 18	IOMUX
Page 19	
Page 20	
Page 21	
Page 22	
Page 23	
Page 24	
Page 25	
Page 26	
Page 26	
Page 27	
Page 28	

1. Unless Otherwise Specified:
- All resistors are in ohms, 10%, 1/8 Watt,0603
- All capacitors are in uF, 20%, 50V,0603
- All voltages are DC
- All polarized capacitors are aluminum electrolytic
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

Revision History

Rev. Code	Date	By	Description
A	2015-02-28	Javen	1 Revision A released
B	2015-07-07	Javen	1 DNP R1023 DNP R1435, R1404, Add R1436 DNP R1517,Install R1520 Change Camera J1801 connector Change JTAG J1902 footprint Change SODIMM J2101 footprint Change R2101 from PU to PD Change J1901 PIN sequence
C	2015-07-14	Javen	1 Add R919-R946,L903-L905 DNP R1436,Install R1404,R1435 Change HP_MIC1N to LINPUT1 Add BT_DISABLE,ECSPI4_SS0,ECSPI4_MOSI,ECSPI4_SCLK for BT Add R2107~R2116 to reduce the VSNVS power consumption due to the TAMPER reason Add L903~L930 as FCC/CE backup Change Camera J1801 connector direction on layout Add C905 Change J1701 from TOP contact to BOT contact for BT
C1	2016-05-05	Javen	1 DNP J1801,J1001 due to cost reason
C2	18-Oct-2016	Marek B.	Updated to be NCL compliance. - parts: J901, J1701, J1802, J2101 - Title blocks

3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



Microcontroller Solutions Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

ICAP Classification: CP: IUO: X PUBI:

Designer:
<Designer>

Drawing Title:
MCIMX6UL-BB

Drawn by:
<DrawnBy>

Page Title:
Title and Rev History

Approved:
<Approver>

Size
C

Document Number
SCH-28616 PDF: SPF-28616

Rev
C2

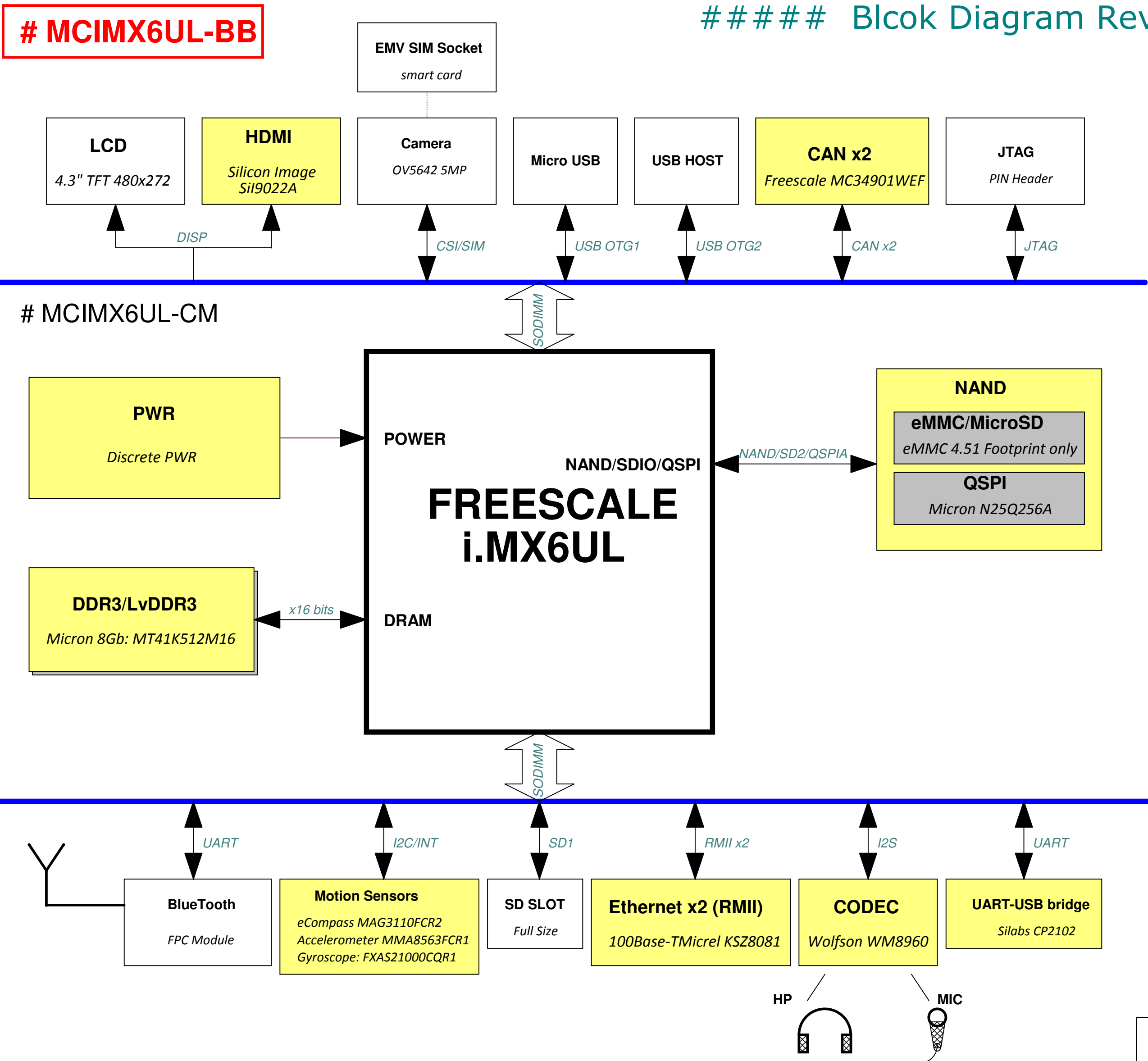
Date: Tuesday, October 18, 2016

Sheet 1 of 18

i.MX6UL EVK Block Diagram

Blcok Diagram Rev 1.0

MPN: MCIMX6UL-BB Agile No: 28616
MPN: MCIMX6UL-CM Agile No: 28617

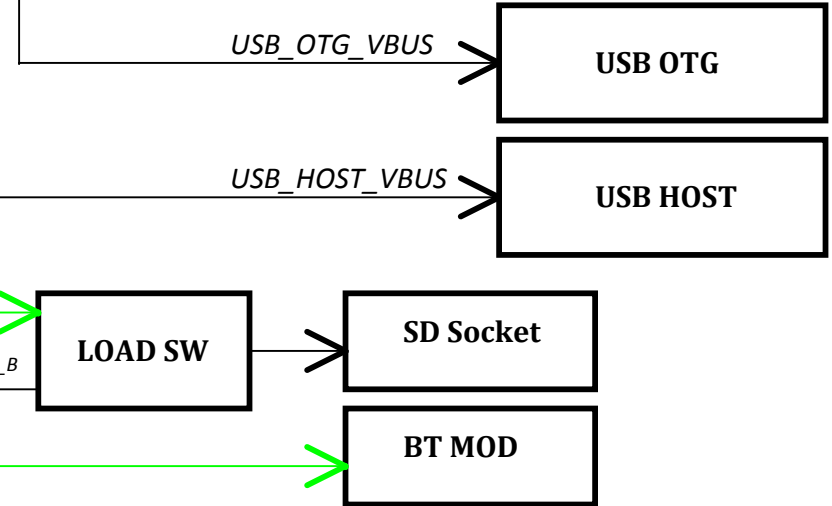
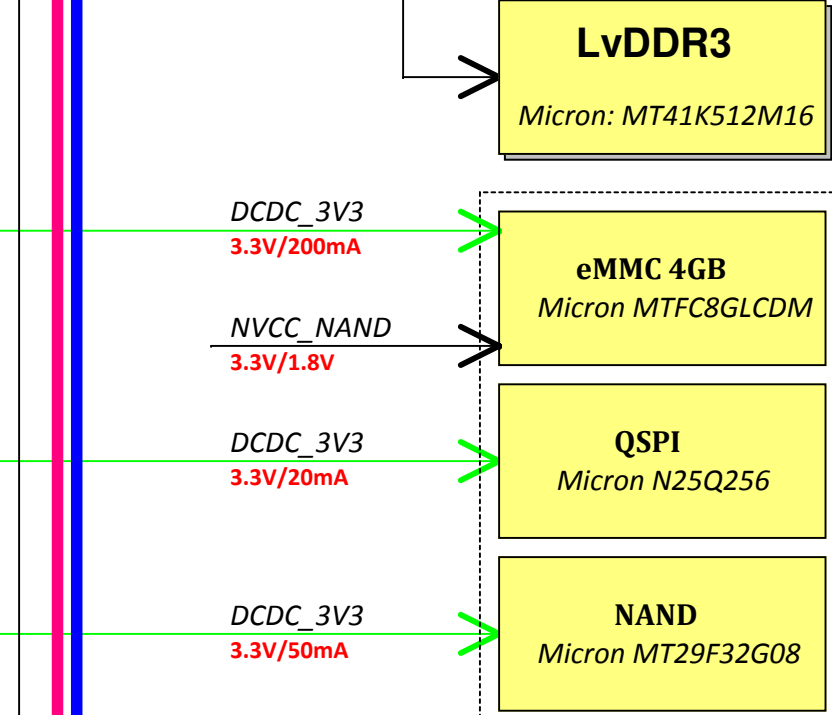
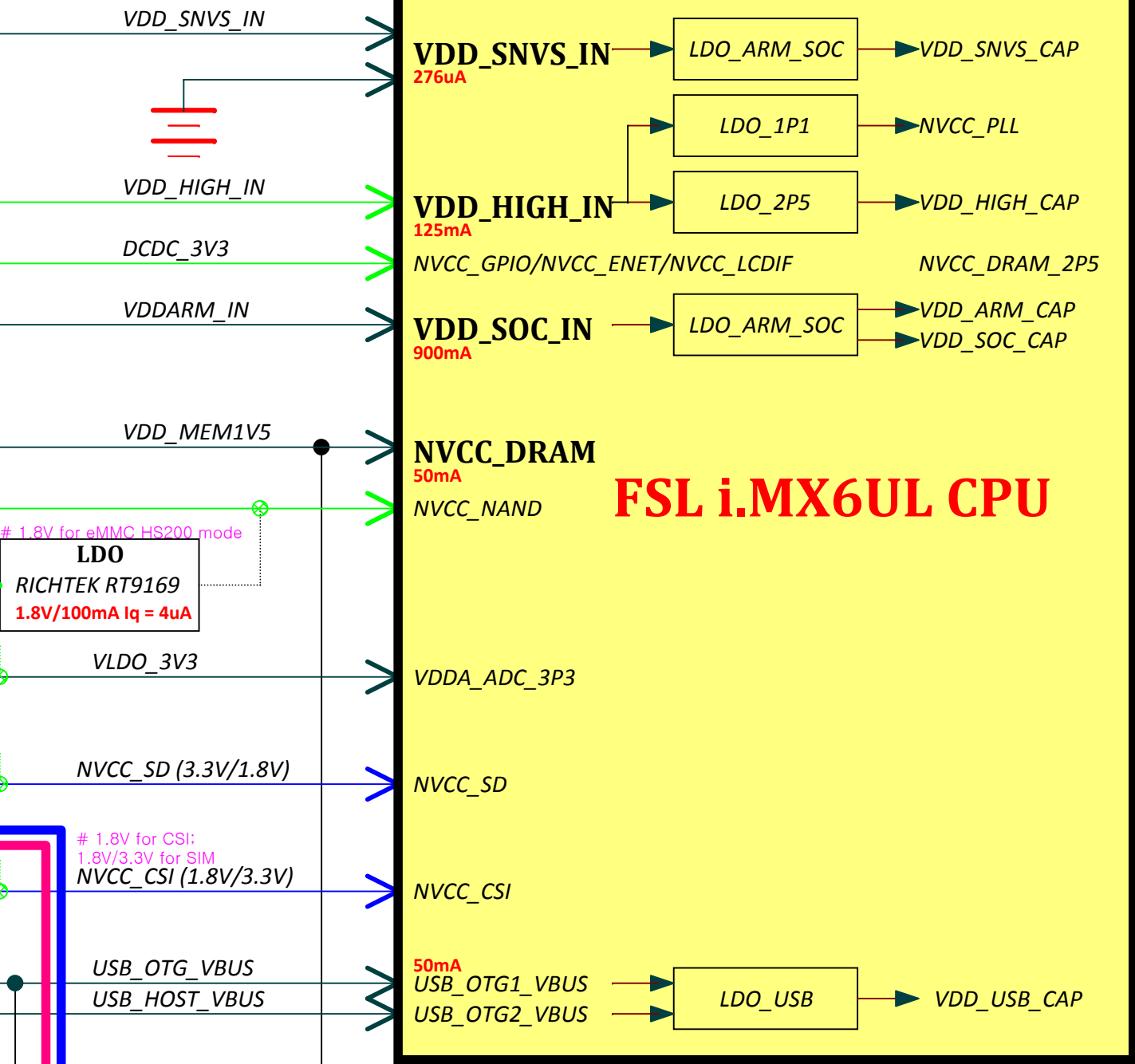
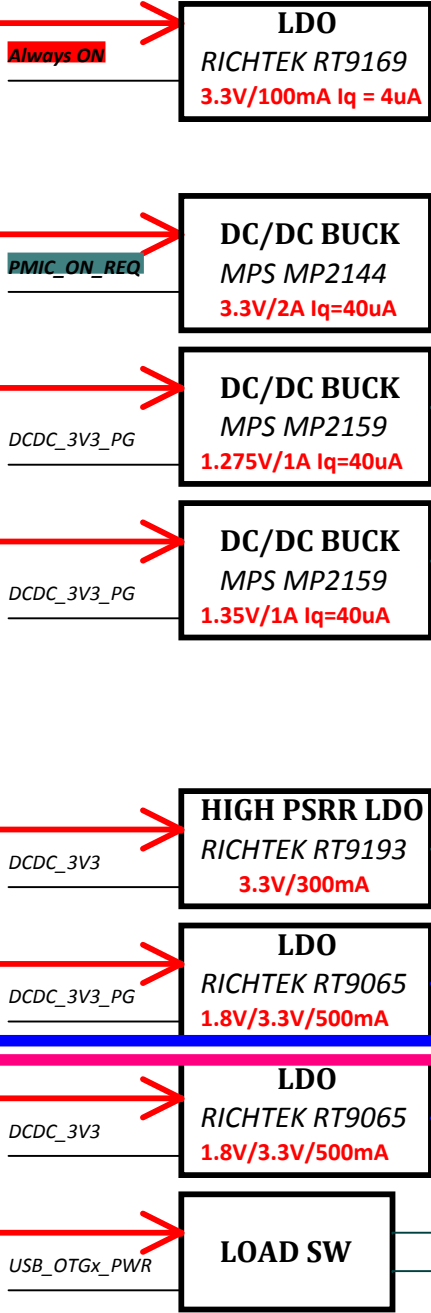
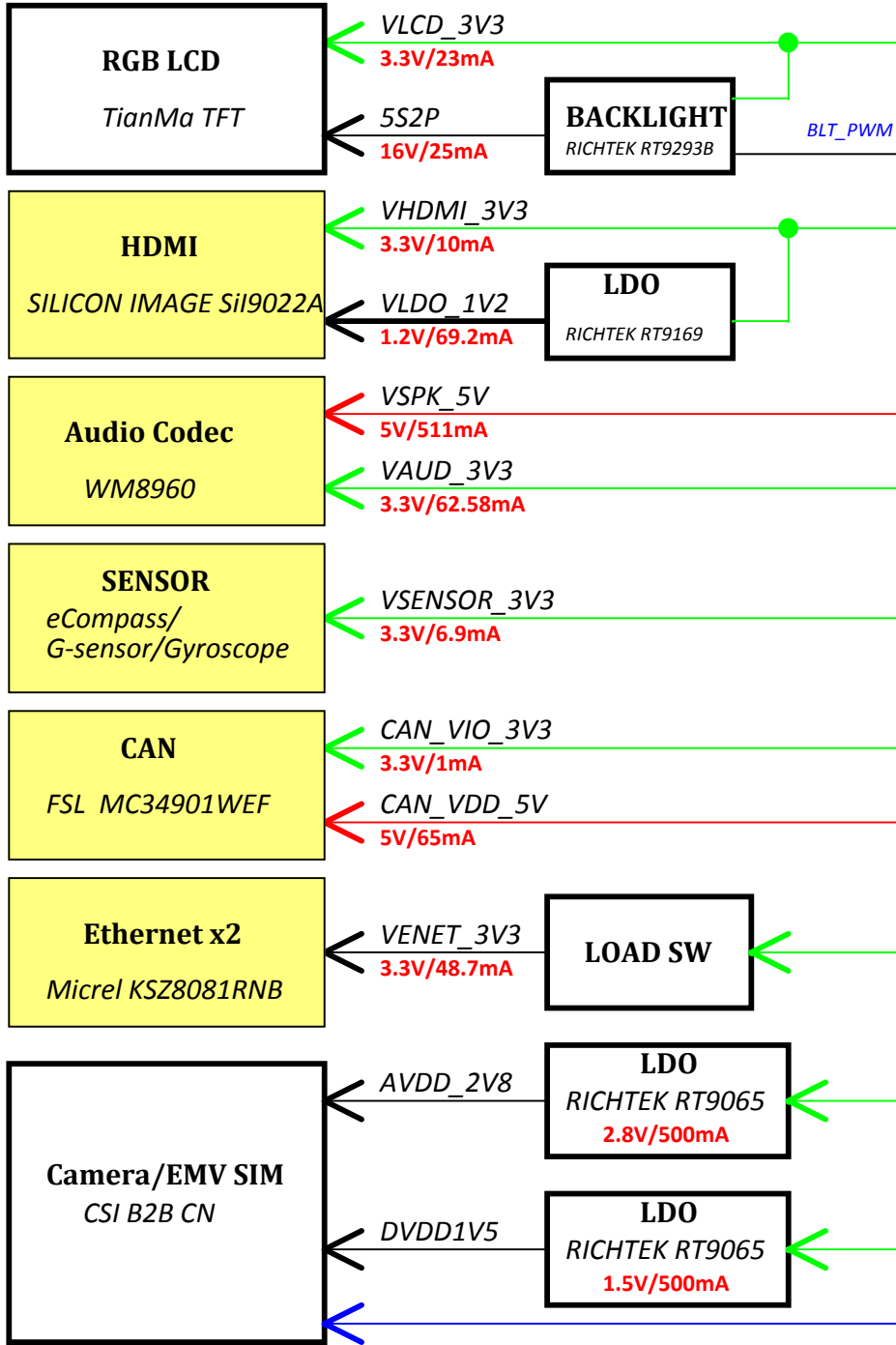


ICAP Classification: CP: IVO: X PUBL:			
Drawing Title: MCIMX6UL-BB			
Page Title: Block Diagram			
Size C	Document Number SCH-28616 PDF: SPF-28616	Rev C2	
Date: Wednesday, October 12, 2016	Sheet 2	of 18	

i.MX6UL EVK PWR TREE

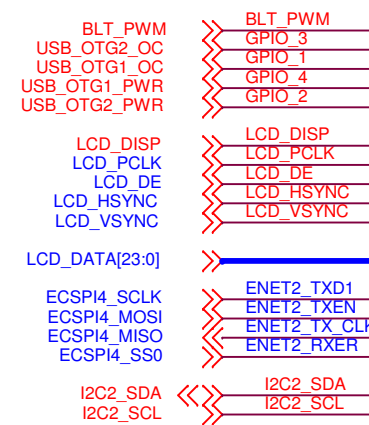
WALL Adapter: 5V/3A

MCIMX6UL-BB



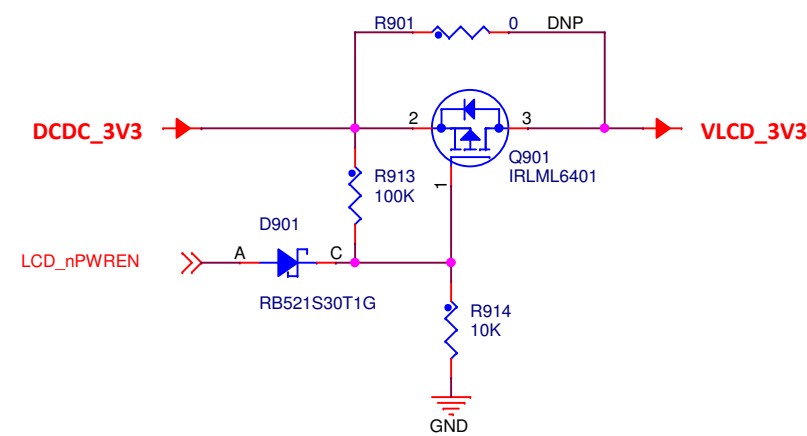
MCIMX6UL-CM

LCD IF

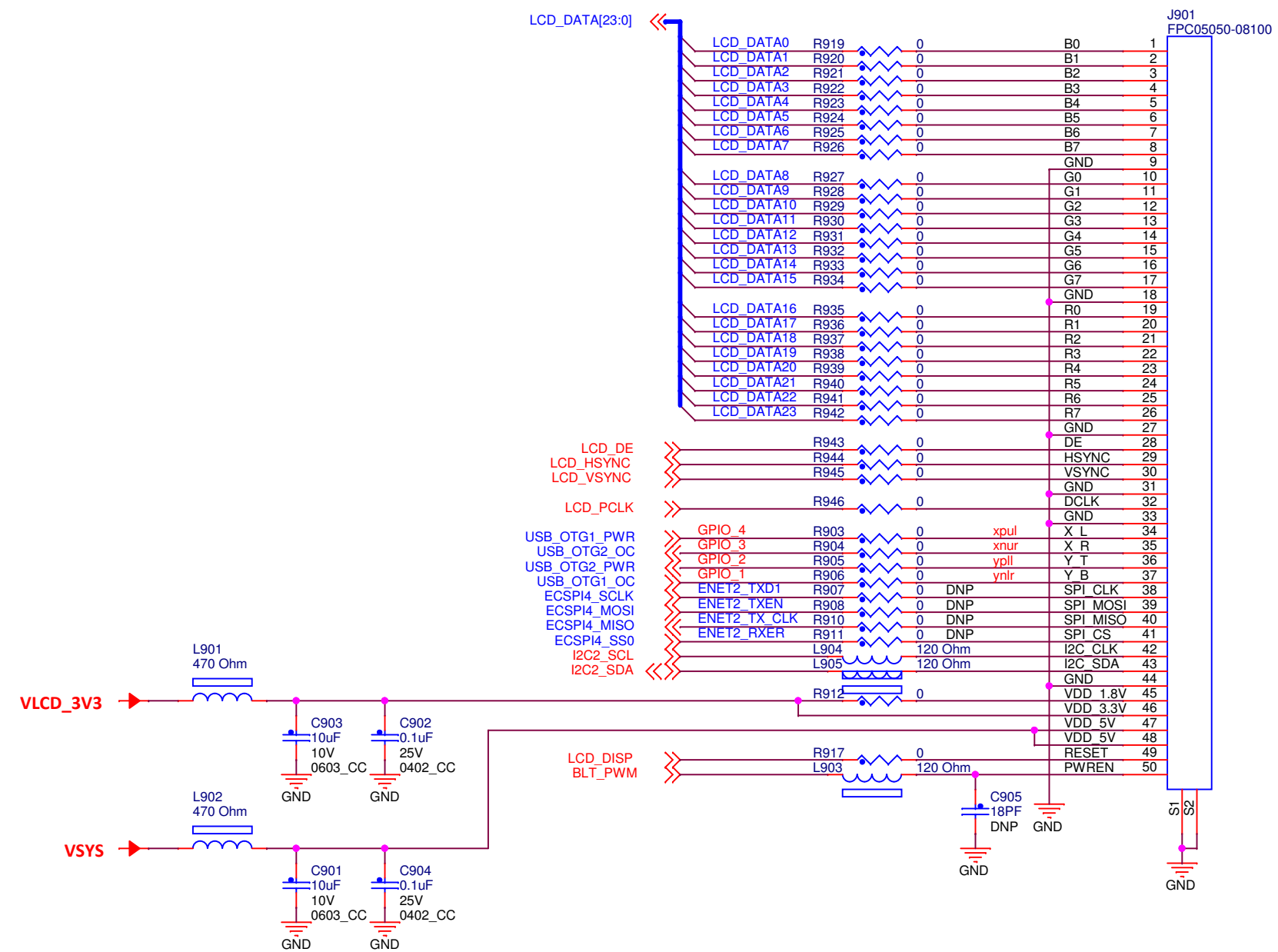


PWR

LCD Standby Mode PWR: 50uW



LCD CN

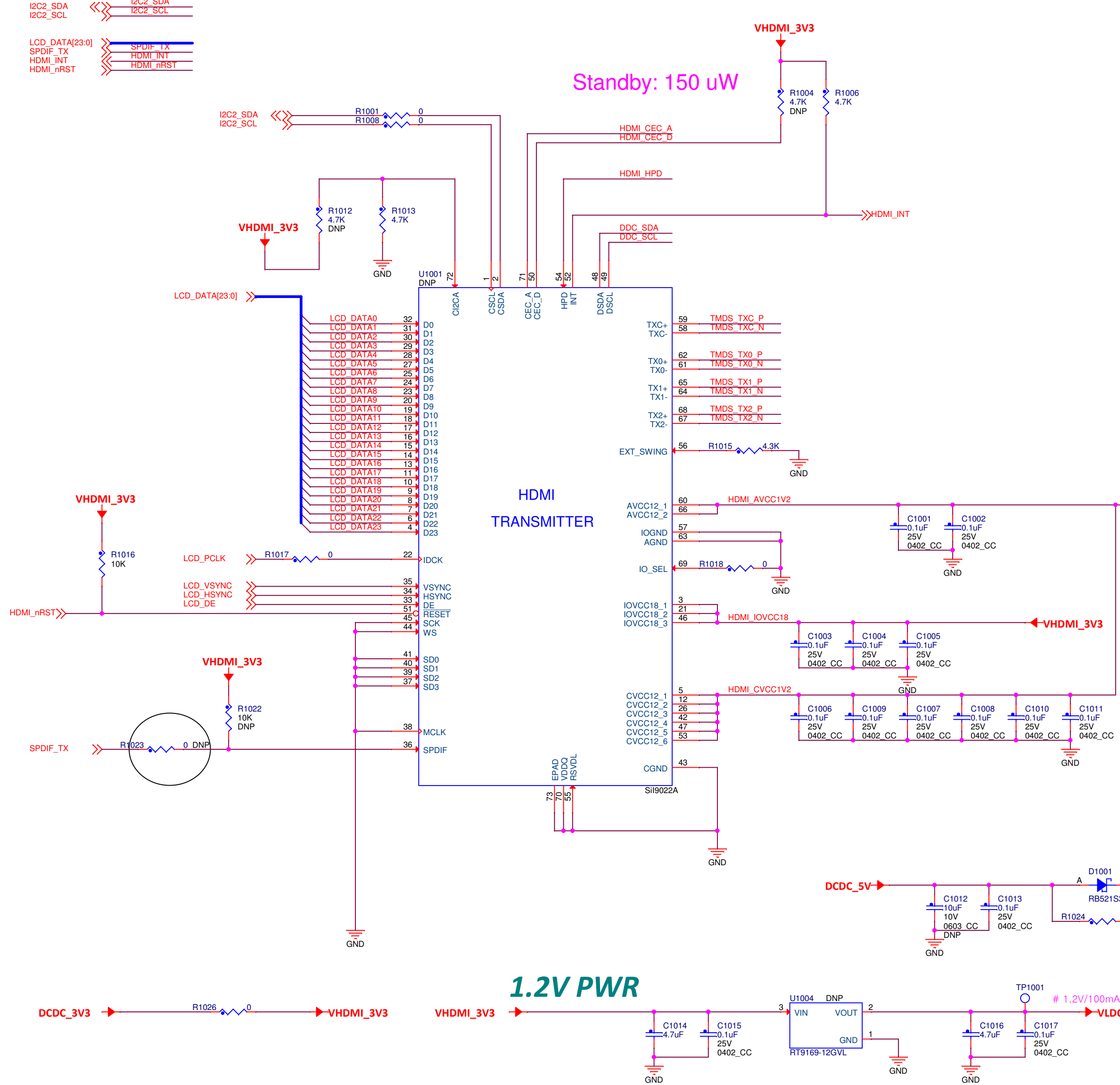
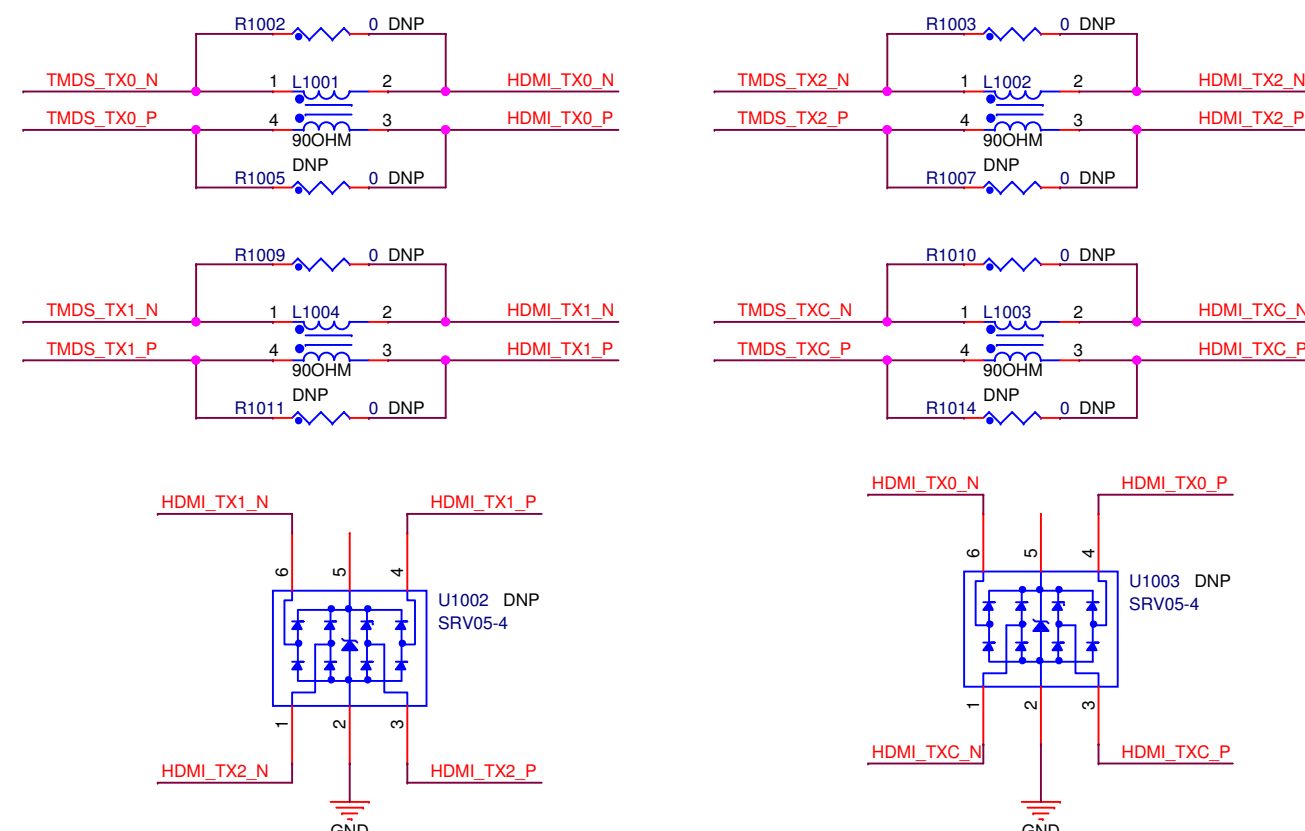


ICAP Classification:	CP:	IUO:	X	PUBI:
Drawing Title:	MCIMX6UL-BB			
Page Title:	LCD			
Size	Document Number	SCH-28616 PDF: SPF-28616	Rev	
C			C2	
Date:	Tuesday, October 18, 2016	Sheet	4	of 18

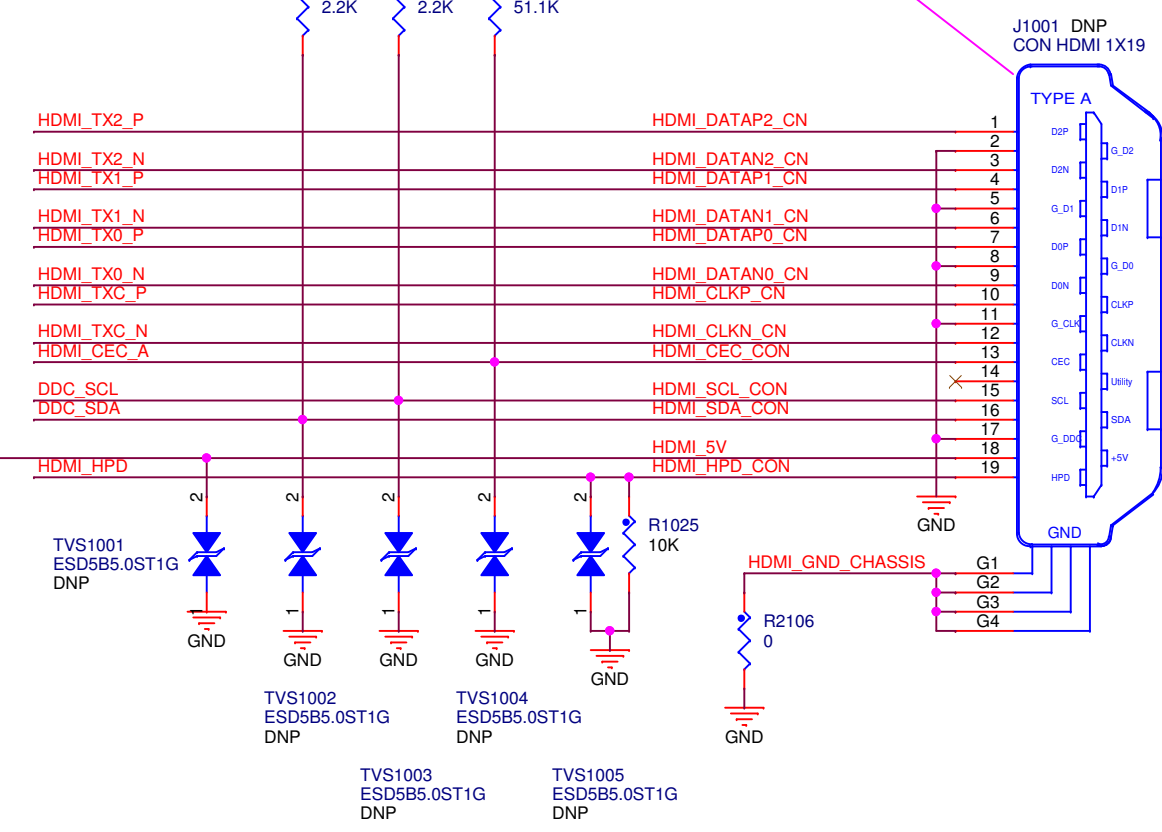
HDMI Transmitter

EMI/ESD

#Res Overlap with EMI Choke



HDMI TYPEA



1.2V PWR

Internal Function	CI2CA = LOW	CI2CA = HIGH
Transmitter Programming Interface (TPI) device address	0x72	0x76
CEC Programming Interface (CPI) device address	0xC0	0xC4
SiI9020-compatible internal registers: first device address	0x72	0x76
SiI9020-compatible internal registers: second device address	0x7A	0x7E

ICAP Classification: CP: IUC: X PUBI:

Drawing Title: MCIMX6UL-BB

Page Title: HDMI

Size C Document Number SCH-28616 PDF: SPF-28616 Rev C2

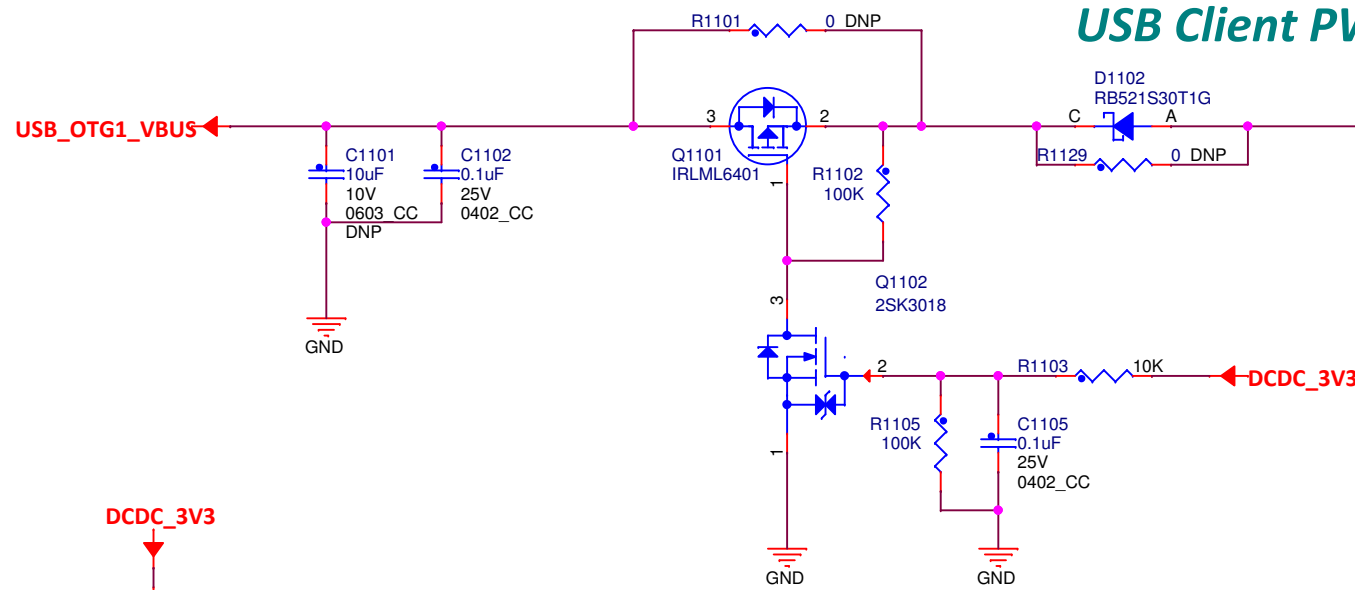
Date: Wednesday, October 12, 2016 Sheet 5 of 18

USB HOST/OTG

USB_OTG1_DN <<< USB_OTG1_DN
USB_OTG1_DP <<< USB_OTG1_DP
USB_OTG2_DN <<< USB_OTG2_DN
USB_OTG2_DP <<< USB_OTG2_DP

USB_OTG1_PWR <<< USB_OTG1_PWR
USB_OTG2_PWR <<< USB_OTG2_PWR
USB_OTG1_ID <<< USB_OTG1_ID
USB_OTG1_OC <<< USB_OTG1_OC
USB_OTG2_OC <<< USB_OTG2_OC

USB Client PWR



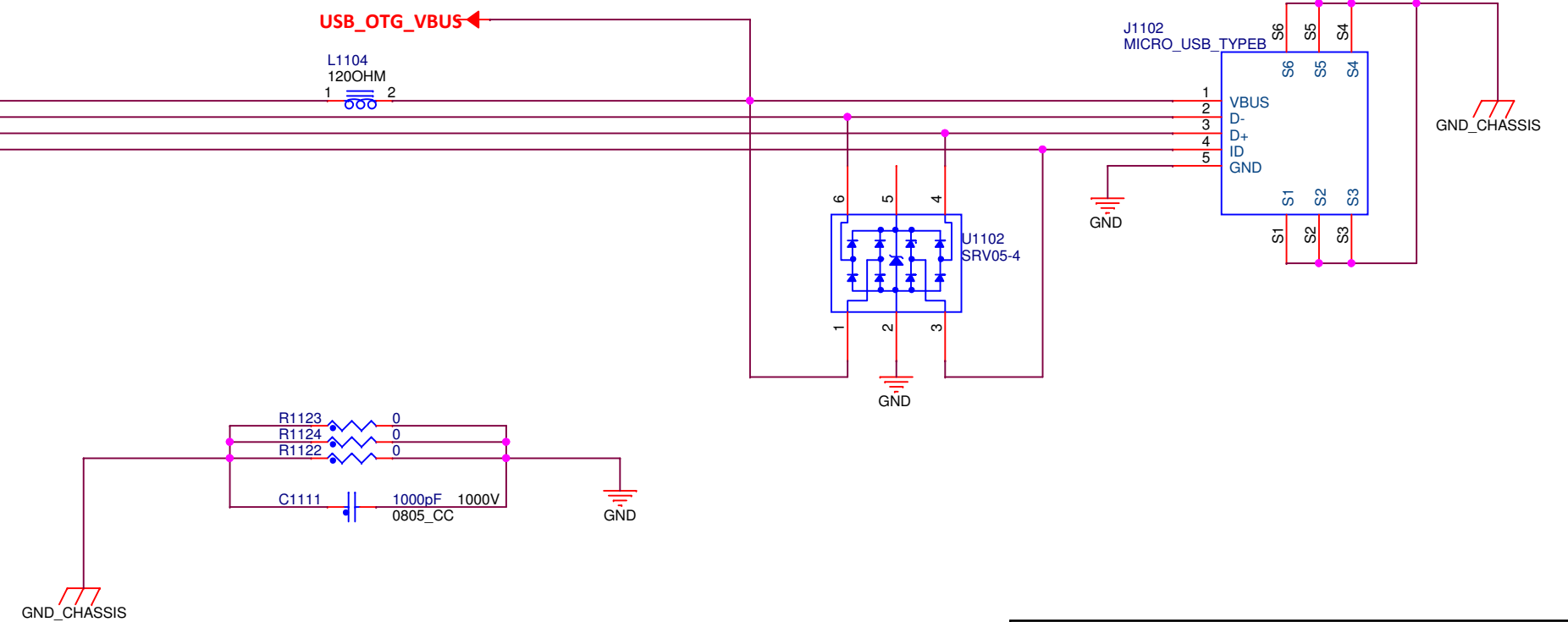
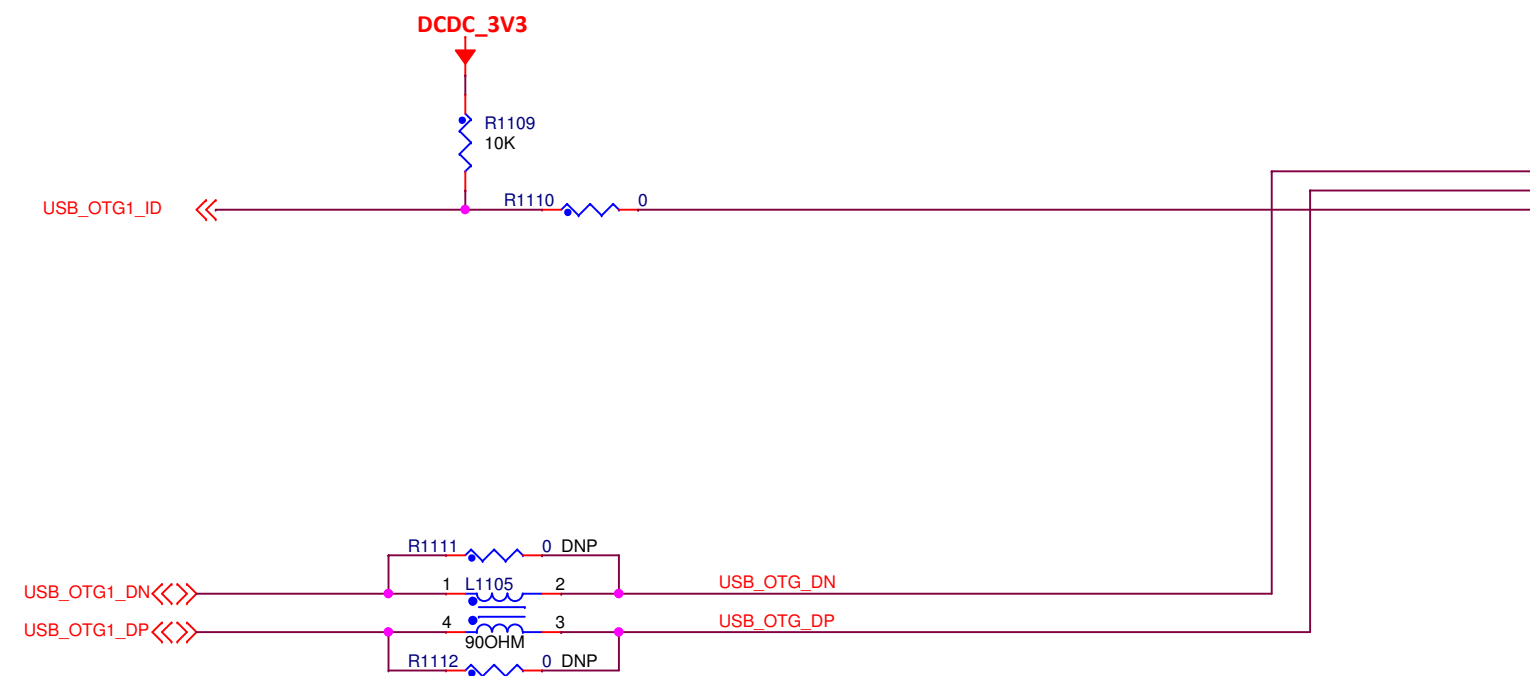
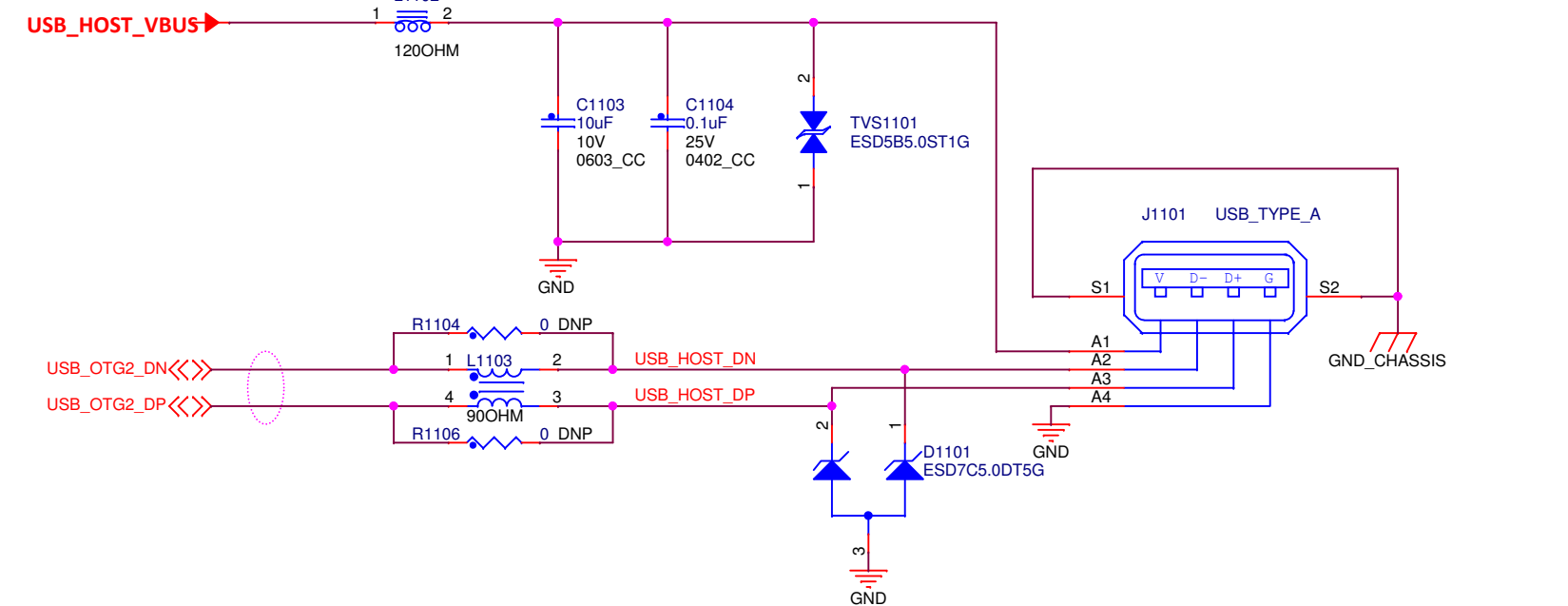
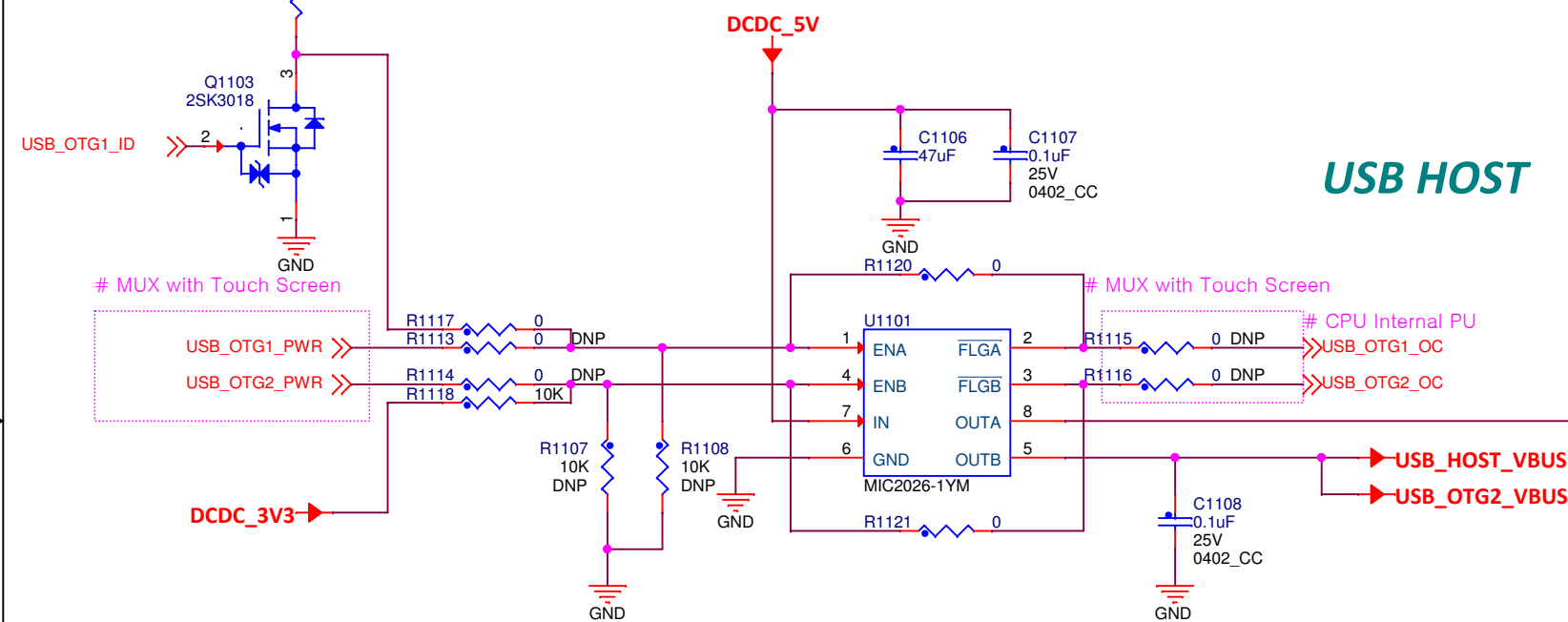
Need to use MIC5225 for ceramic output cap.

Max output current from MIC5225 is 150mA

$V_o = 1.24V \times (1 + R_a/R_b)$

This block is reserved for USB OTG certification test.

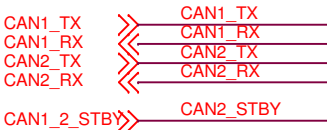
USB HOST



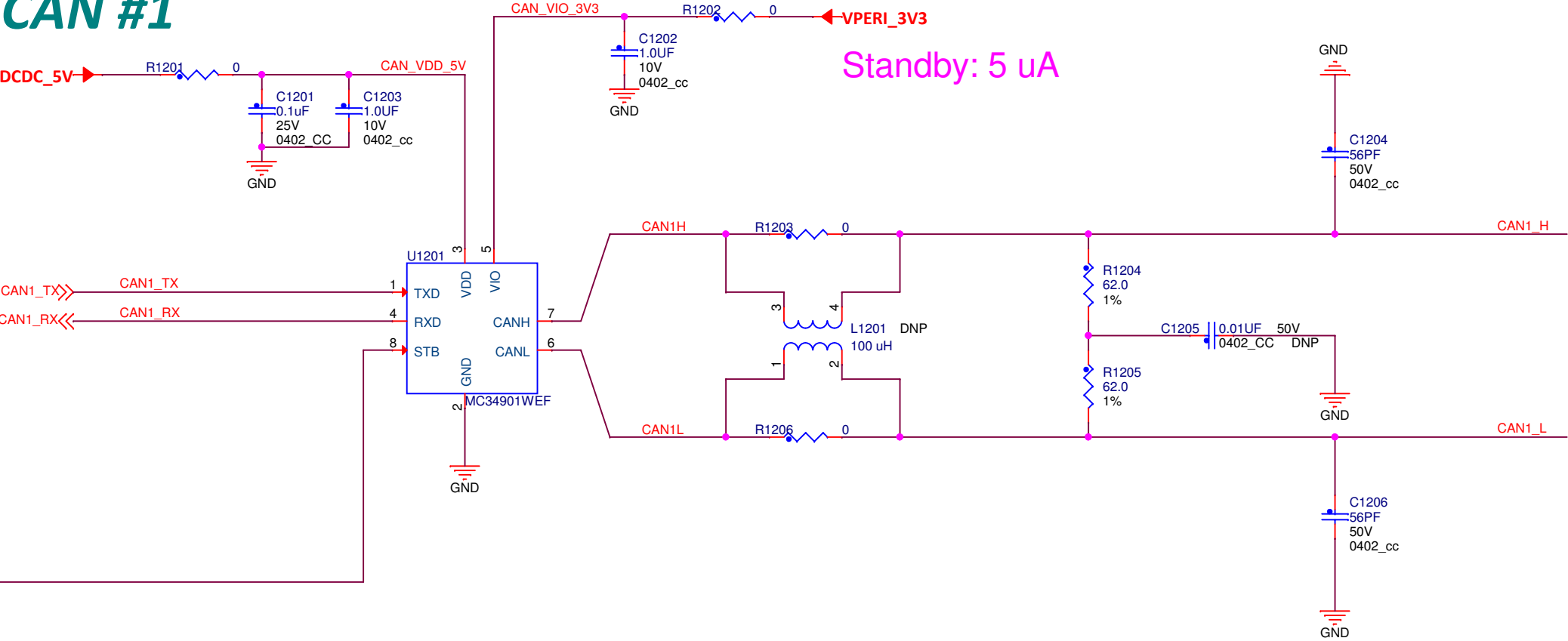
ICAP Classification:	CP:	IUO:	X	PUBI:
Drawing Title:	MCIMX6UL-BB			
Page Title:	USB			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2	
Date:	Wednesday, October 19, 2016	Sheet 6	of 18	

High Speed CAN Transceiver

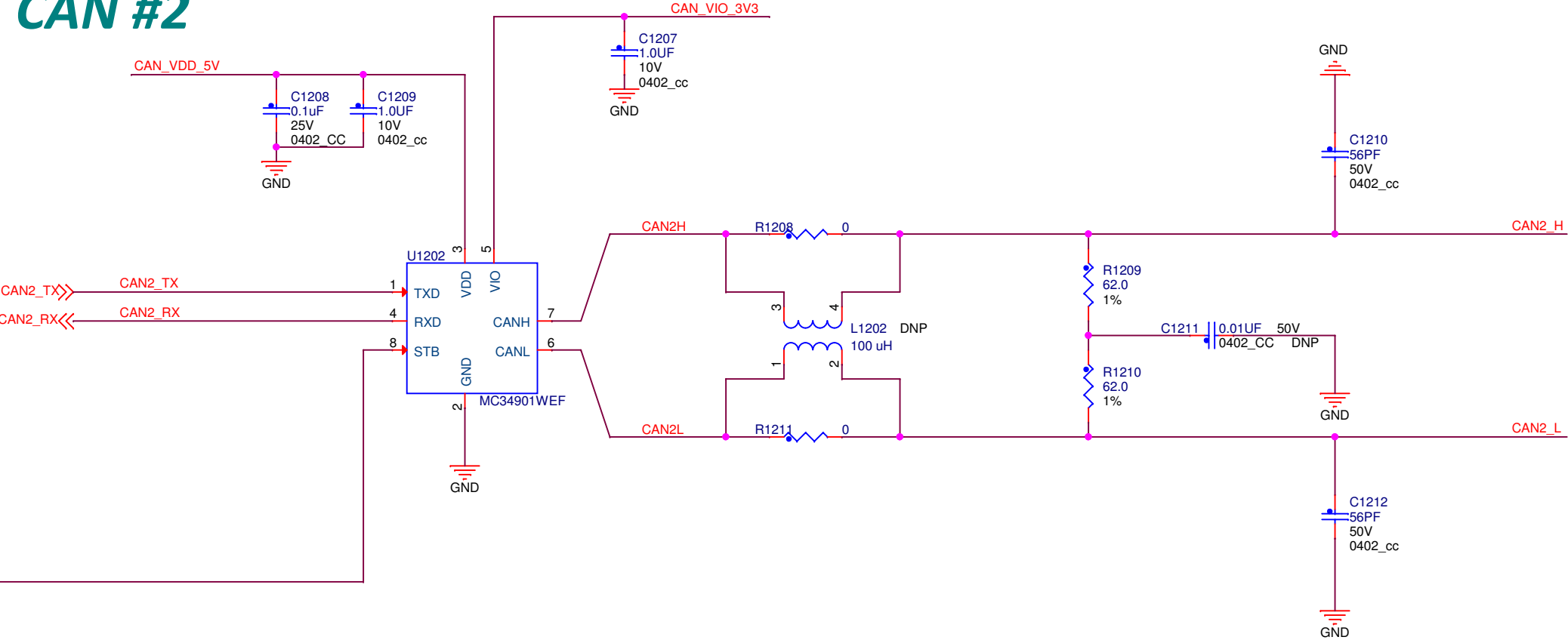
FSL High Speed CAN Transceiver



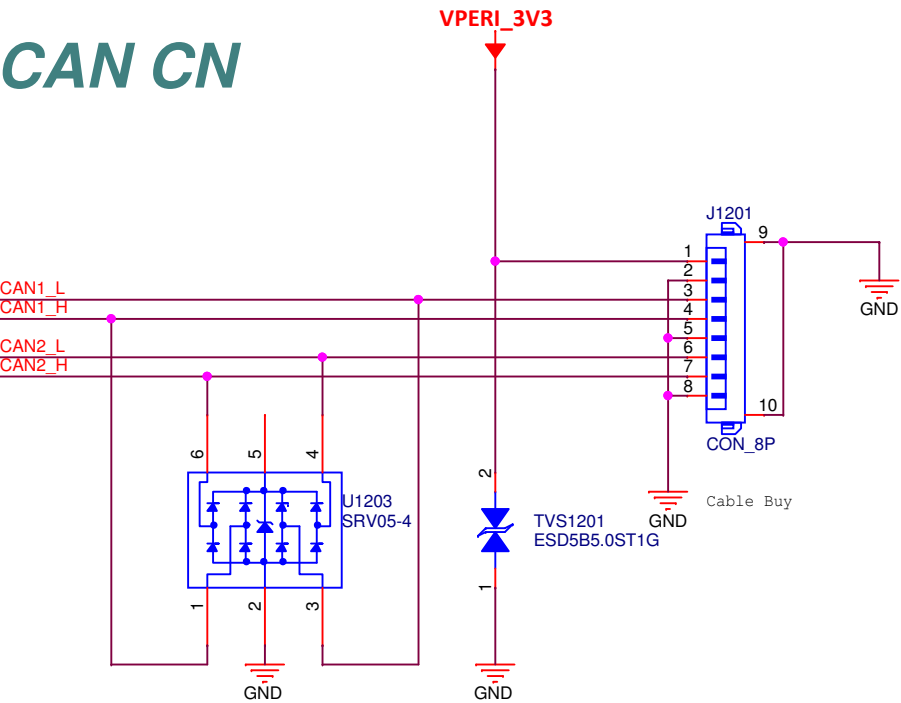
CAN #1



CAN #2



CAN CN



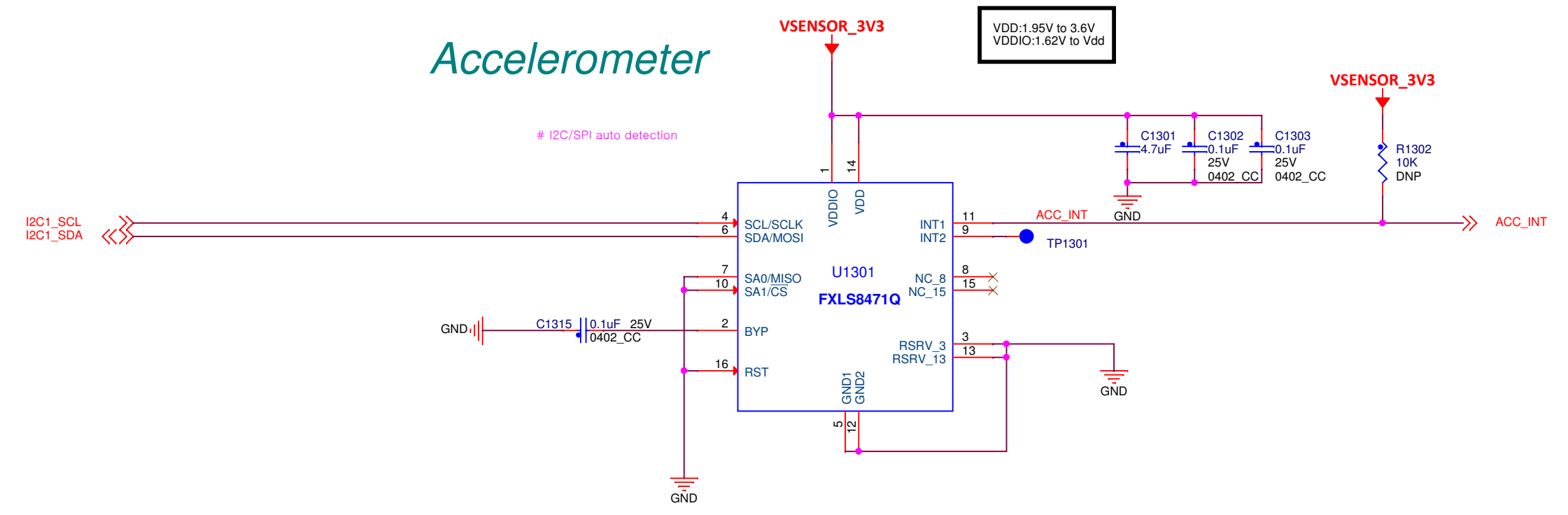
ICAP Classification: CP: IVO: X PUBL:			
Drawing Title: MCIMX6UL-BB			
Page Title: CAN			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2
Date:	Wednesday, October 12, 2016	Sheet 7	of 18

Motion Sensor 9-axis

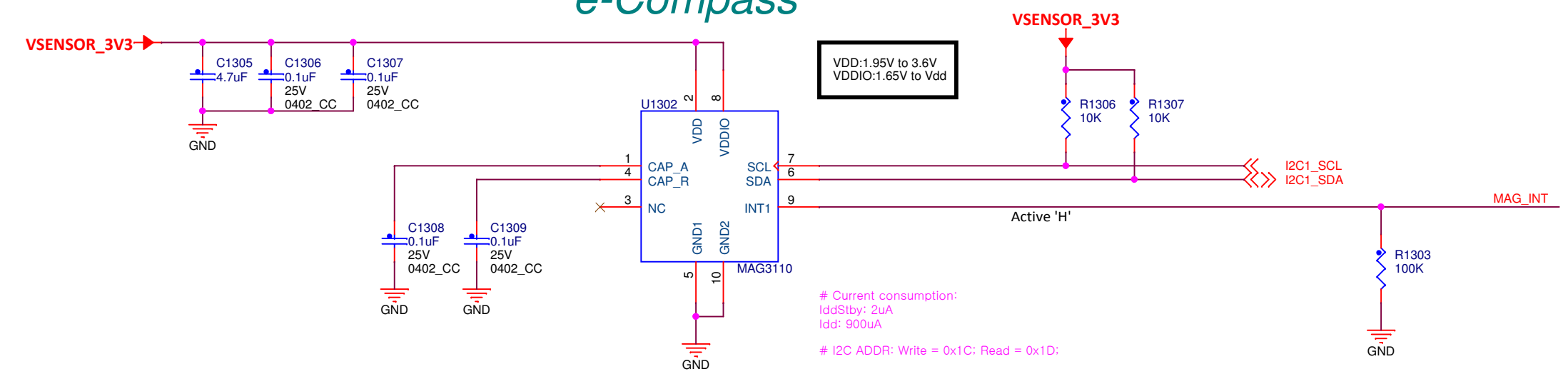
I2C1_SDA
I2C1_SCL
ACC_INT

VPERI_3V3 → R1301 0 → VSENSOR_3V3

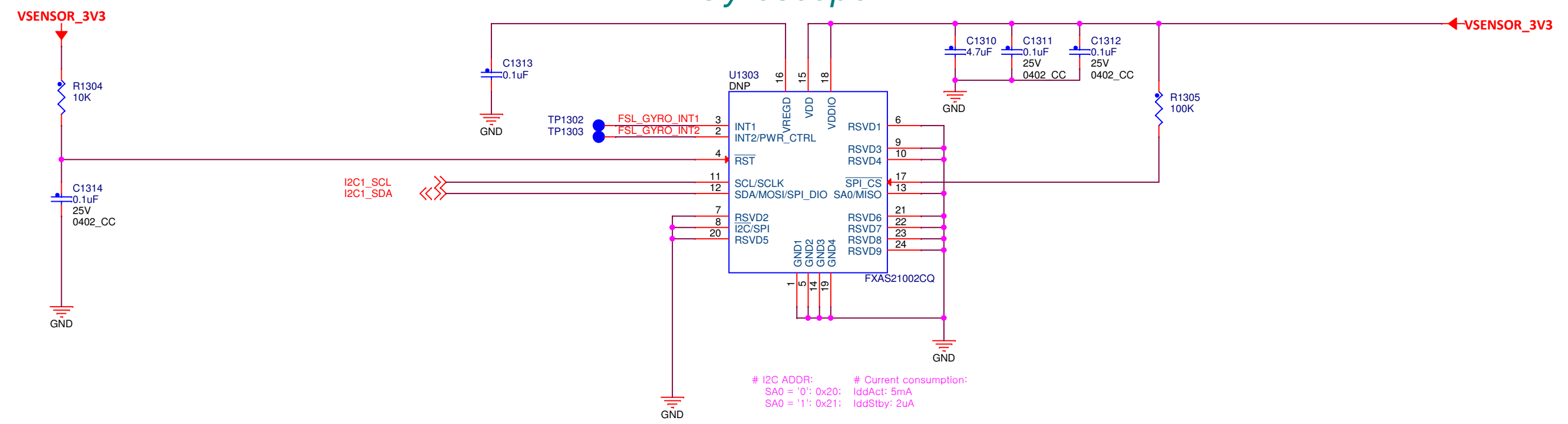
Accelerometer



e-Compass



Gyroscope



ICAP Classification: CP: IVO: X PUBI:			
Drawing Title: MCIMX6UL-BB			
Page Title: Sensor			
Size C	Document Number	SCH-28616 PDF: SPF-28616	Rev C2
Date:	Wednesday, October 12, 2016	Sheet 8 of 18	

Audio Codec

I2C2_SDA <<> I2C2_SDA
I2C2_SCL <<> I2C2_SCL
SAI2_SYNC <<> SAI2_SYNC
SAI2_BCLK <<> SAI2_BCLK
SAI2_RXD <<> SAI2_RXD
SAI2_TXD <<> SAI2_TXD
SAI2_MCLK <<> SAI2_MCLK
AUD_INT <<> AUD_INT

VPERI_3V3

Codec

OFF, SLEEP MODE

DCVDD 1.71V - 3.6V
DBVDD 1.71V - 3.6V
AVDD 2.70V - 3.6V
SPKVDD 2.70V - 5.5V

HP JACK

HP_DET:
LOW : REMOVE
HIGH : PLUG

Main Board MIC

HP MIC

SPK

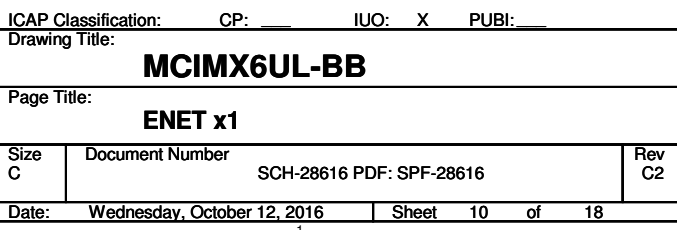
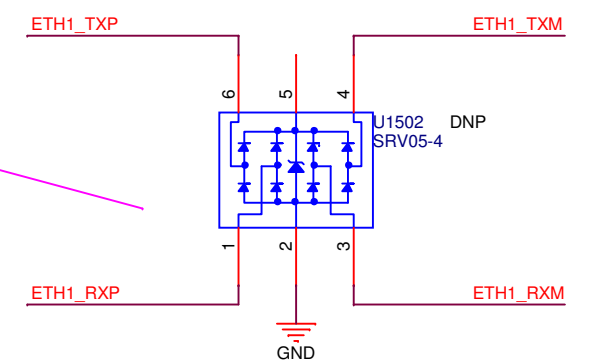
ENET_MDIO	⏏	ENET MDIO
ENET_MDC	⏏	ENET1_MDC
ENET1_TXD0	⏏	ENET1_TXD0
ENET1_TXD1	⏏	ENET1_TXD1
ENET1_TXEN	⏏	ENET1_TXEN
ENET1_TX_CLK	⏏	ENET1_TX_CLK
ENET1_RXD0	⏏	ENET1_RXD0
ENET1_RXD1	⏏	ENET1_RXD1
ENET1_RXER	⏏	ENET1_RXER
ENET1_CRS_DV	⏏	ENET1_CRS_DV
ENET1_nINT	⏏	ENET1_nINT
ENET1_nRST	⏏	ENET1_nRST



The schematic shows the VENET_3V3 power supply network connected to GND. It includes pull-up resistors (R1516-R1527) for PHY addresses (ENET1_PHYAD0-2), configuration bits (ENET1_CONFIG0-2), isolate mode (ENET1_ISO), LED/NWAYEN, duplex/speed (ENET1_LED1/SPEED), broadcast-off (ENET1_B-CAST-OFF), and NAND tree enable (ENET1_NAND_TREE#). The values are specified as 4.7K or 1K, with DNP indicating no pull-down.

# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00001 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (defaule) = Disable
SPEED	SPEED mode Pull-up (defaule) = 100Mbps Pull-down = 10Mbps

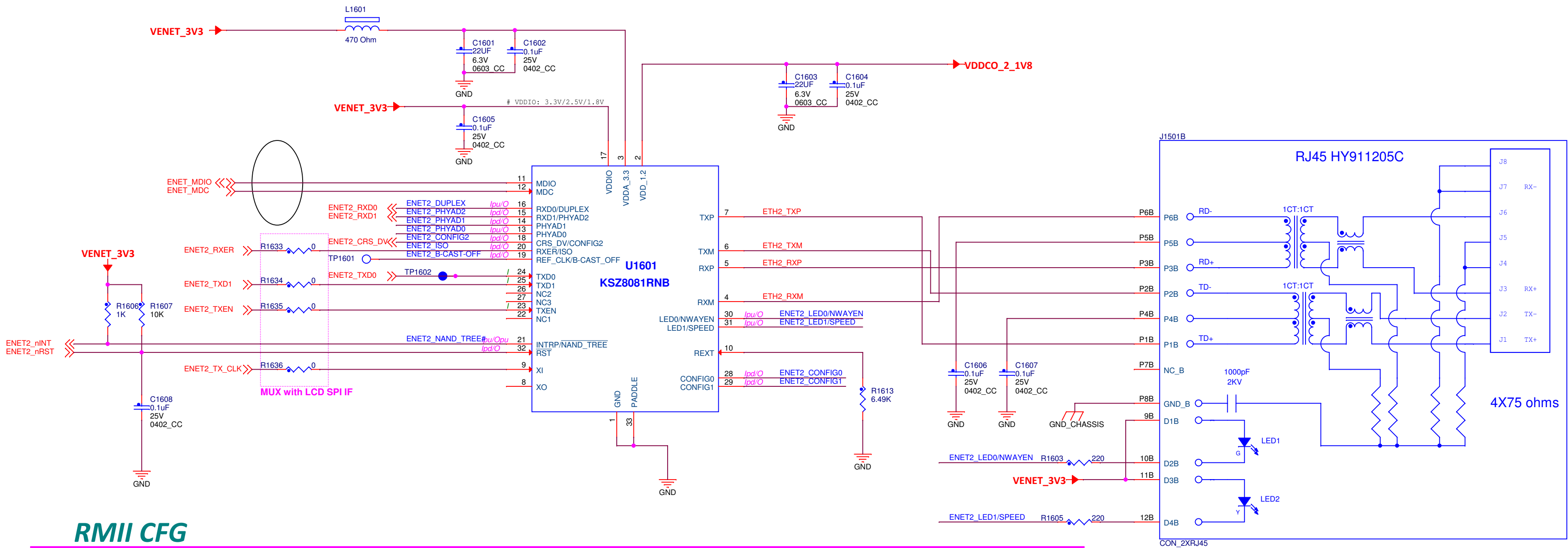
# CFG	Description
DUPLEX	DUPLEX mode Pull-up (defaule) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (defaule) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (defaule) = Disable Pull-down = Enable



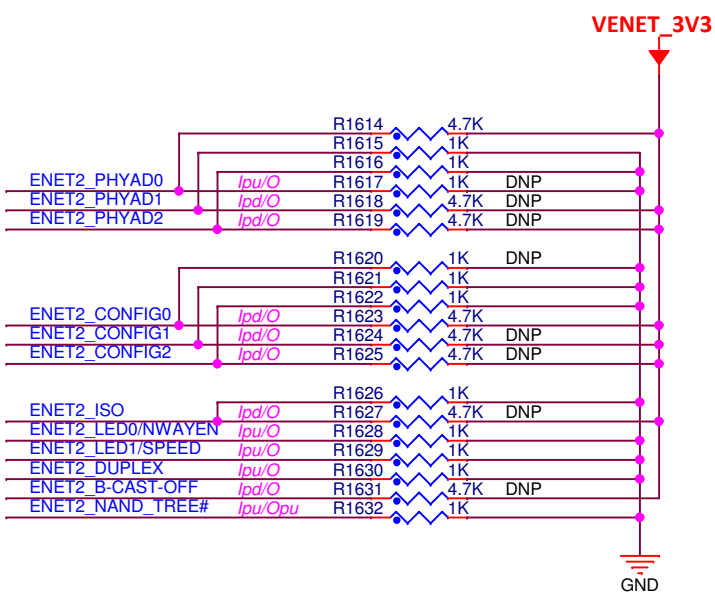
100M ETHERNET RMII PHY x2

ENET_MDIO <<> ENET_MDIO
ENET_MDC <<> ENET_MDC
ENET2_TXD0 <<> ENET2_TXD0
ENET2_TXD1 <<> ENET2_TXD1
ENET2_TXEN <<> ENET2_TXEN
ENET2_TX_CLK <<> ENET2_TX_CLK
ENET2_RXD0 <<> ENET2_RXD0
ENET2_RXD1 <<> ENET2_RXD1
ENET2_RXER <<> ENET2_RXER
ENET2_CRS_DV <<> ENET2_CRS_DV

ENET2_nINT <<> ENET2_nINT
ENET2_nRST <<> ENET2_nRST



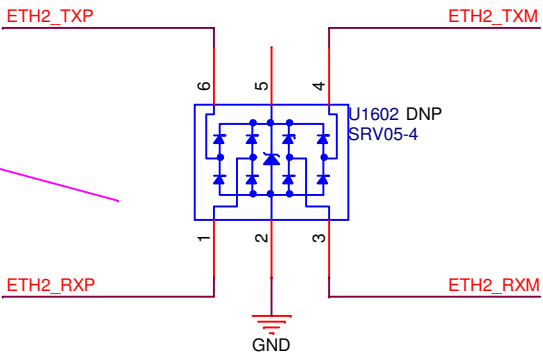
RMII CFG



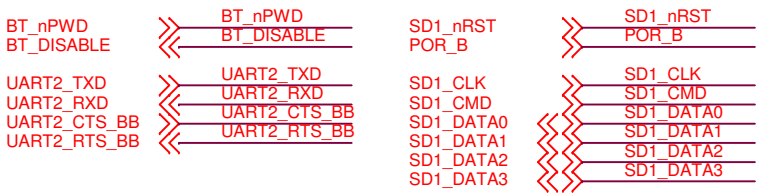
# CFG	Description	# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00001 DEFAULT)	DUPLEX	DUPLEX mode Pull-up (defaule) = Half Duplex Pull-down = Full Duplex
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used	NWAYEN	Nway Auto-Negotiation Pull-up (defaule) = Enable Pull-down = Disable
ISO	ISOLATE mode Pull-up = Enable Pull-down (defaule) = Disable	B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
SPEED	SPEED mode Pull-up (defaule) = 100Mbps Pull-down = 10Mbps	NAND_TREE#	NAND Tree Mode Pull-up (defaule) = Disable Pull-down = Enable

ESD PROTECTION

2rd LEVEL ESD



BLUETOOTH / SD FULL SOCKET

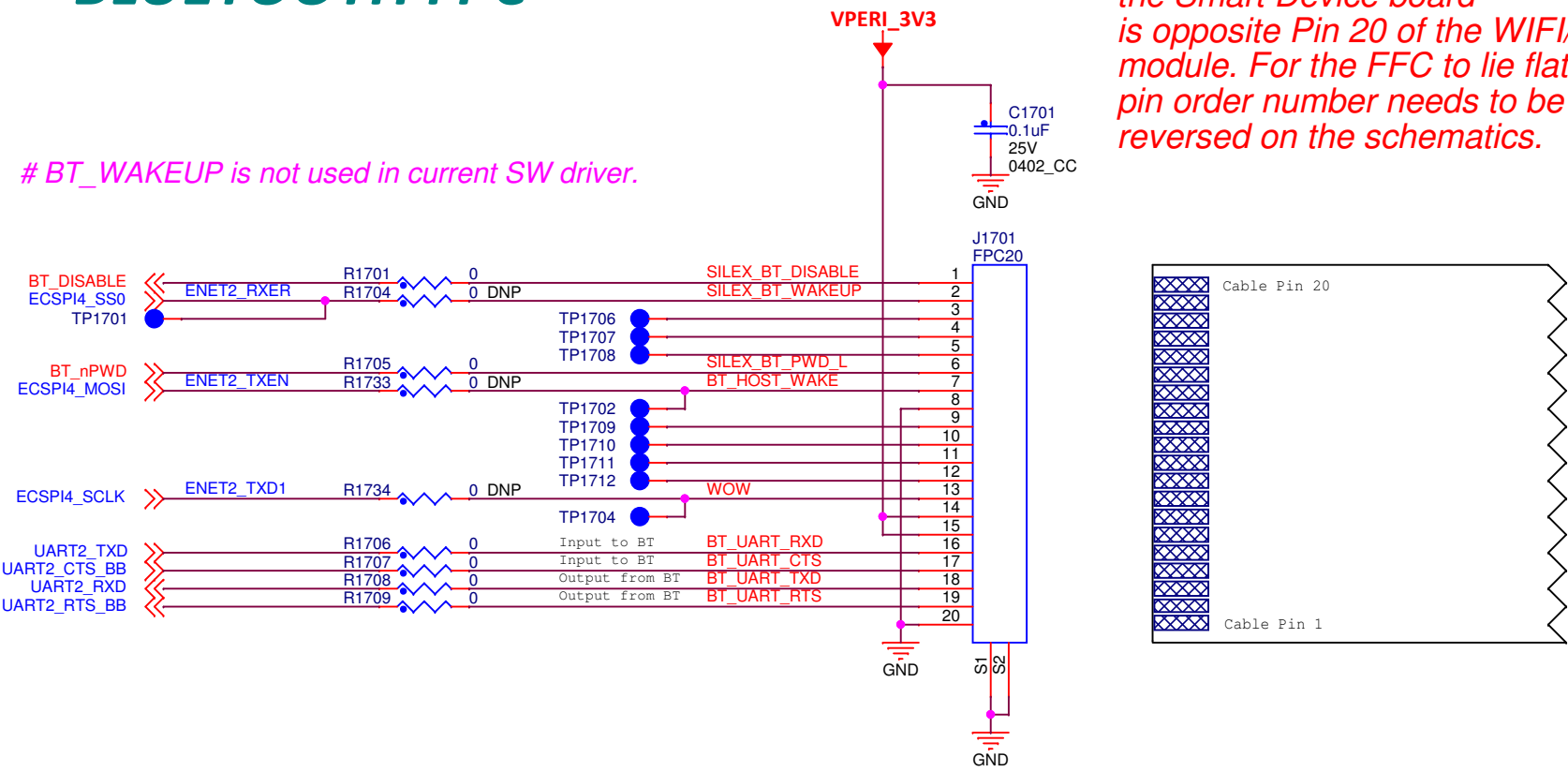


NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT. Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

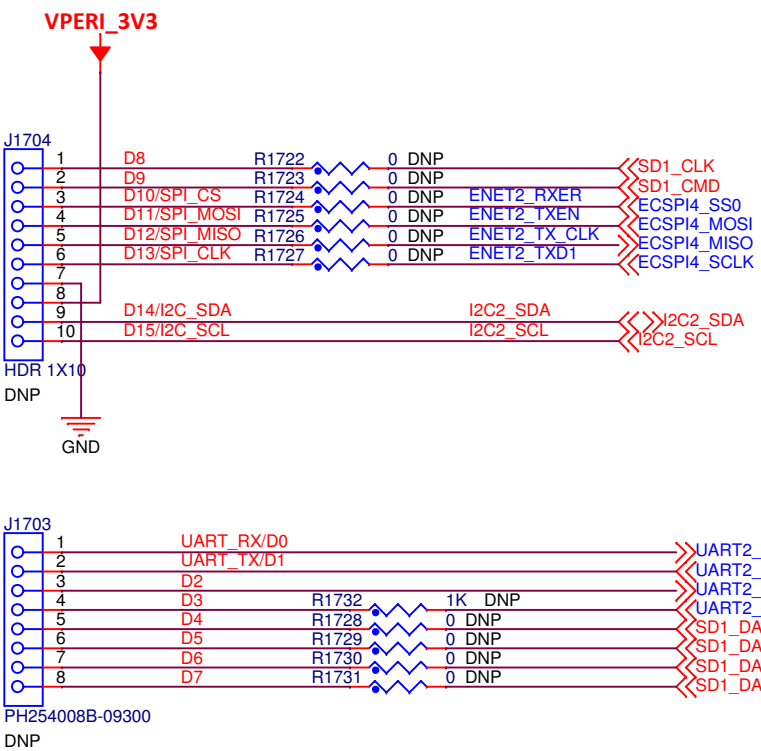
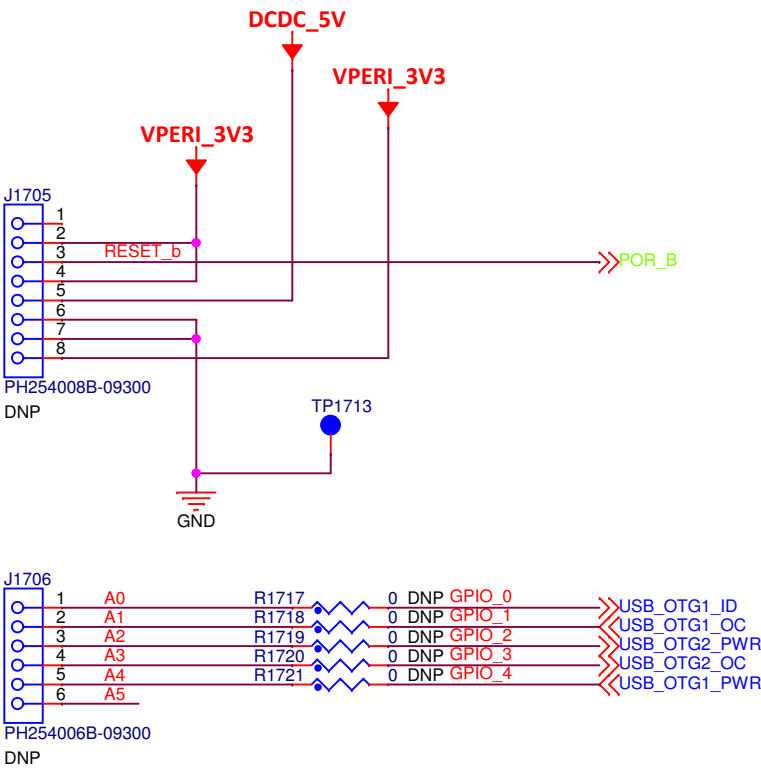
NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

BLUETOOTH FPC

BT_WAKEUP is not used in current SW driver.

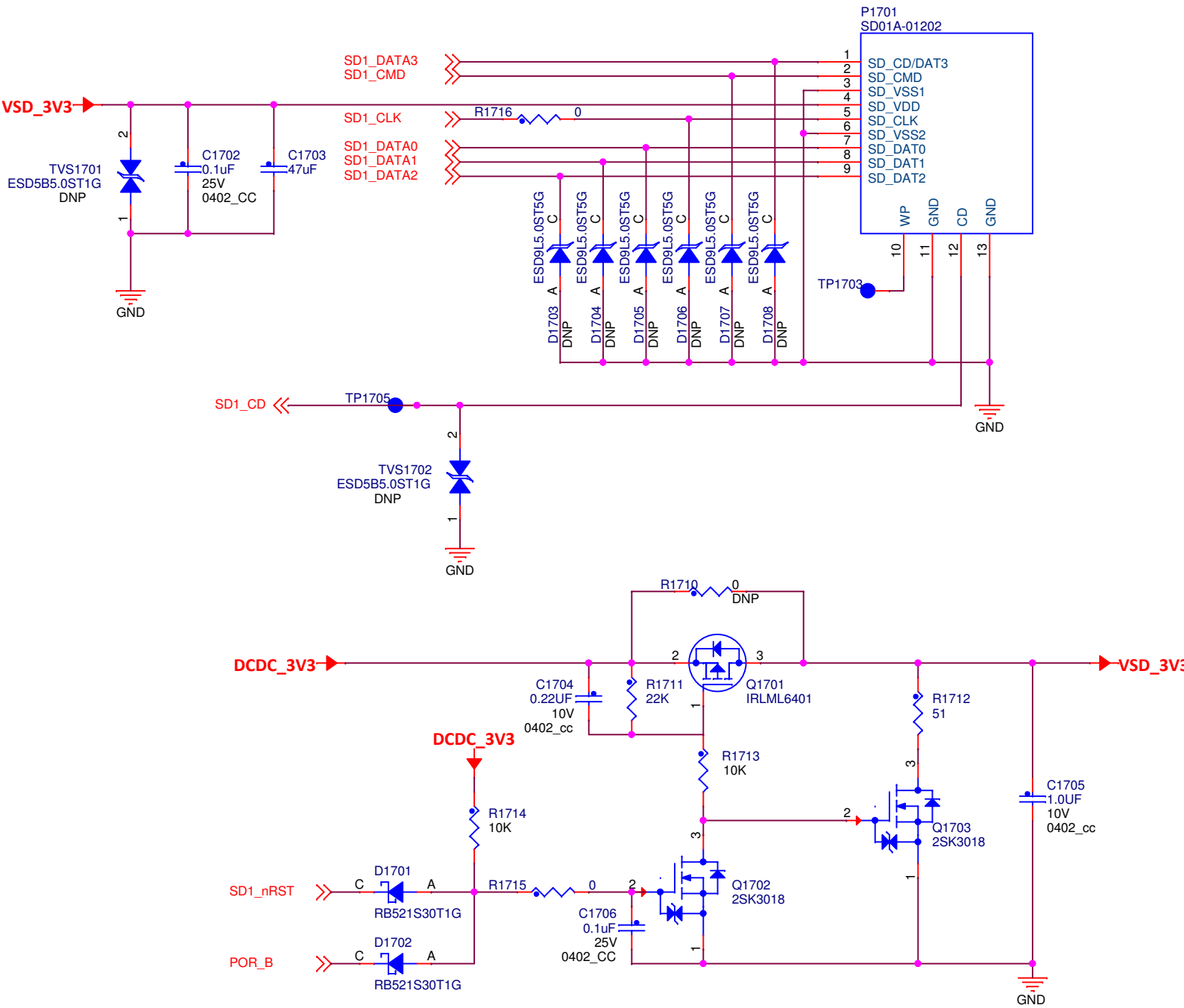


ARDUINO_HEADERS



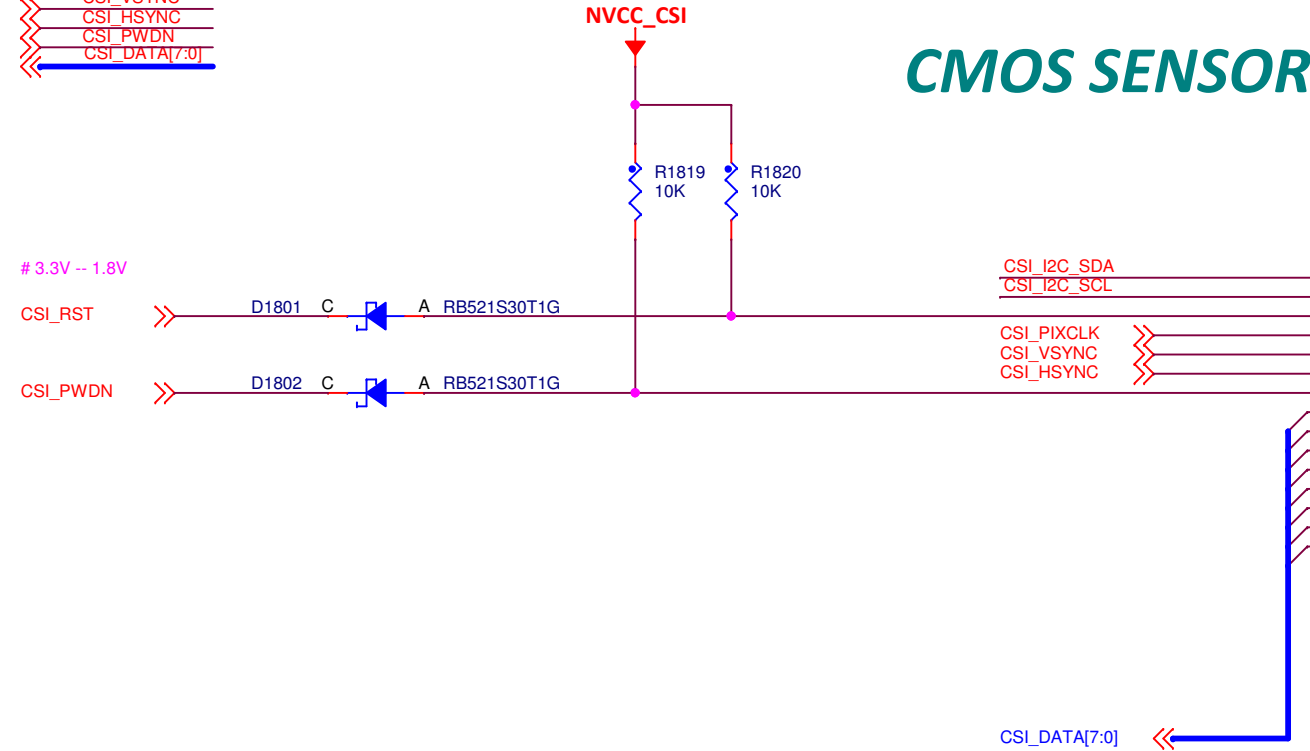
SD SLOT

for WiFi and SD Accessories



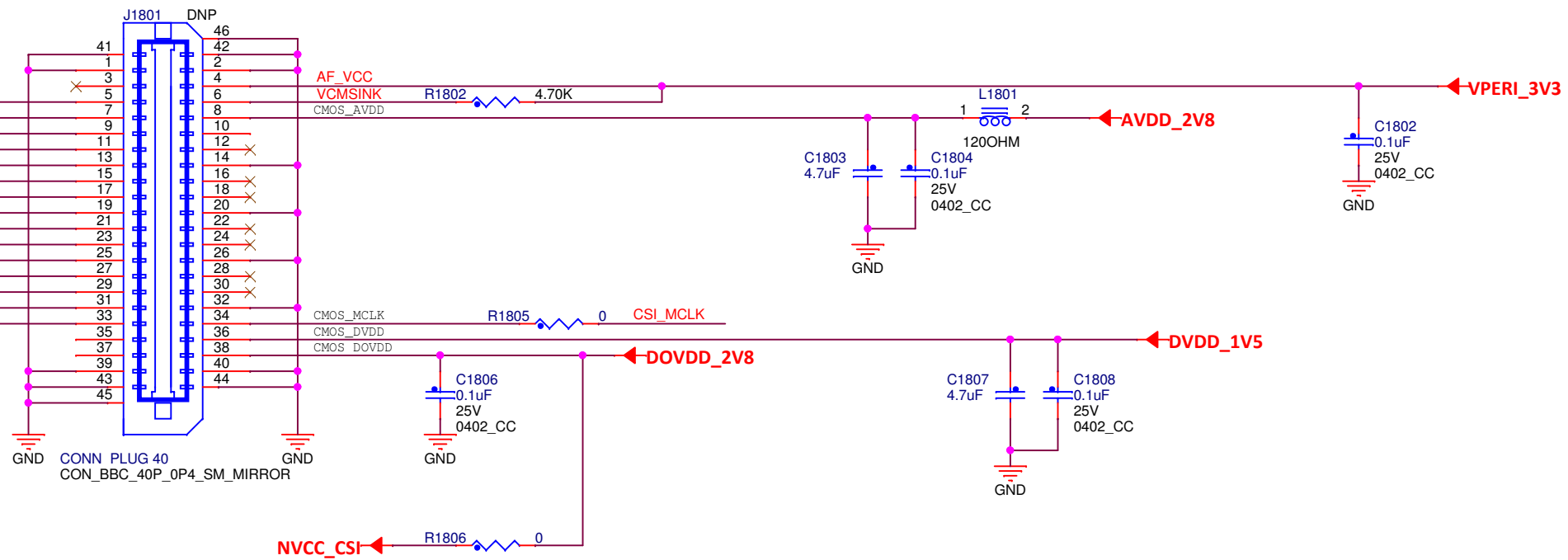
Camera / SIM

I2C2_SDA
I2C2_SCL
CSI_RST
CSI_MCLK
CSI_PIXCLK
CSI_VSYNC
CSI_HSYNC
CSI_PWDN
CSI_DATA[7:0]



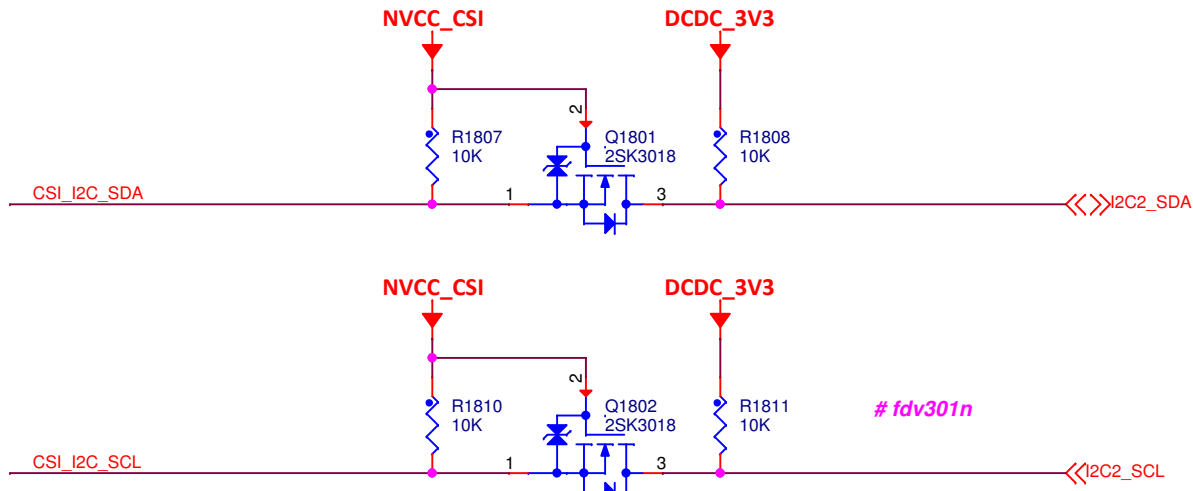
CMOS SENSOR

OV5640 5MP

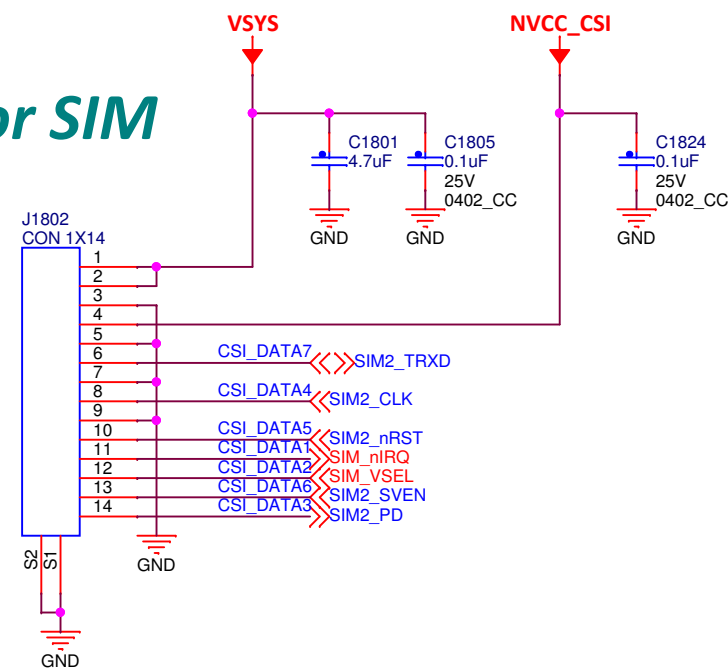


Use Omnivision OV5640/5642 5M Pixel Sensor with this connector (not included)

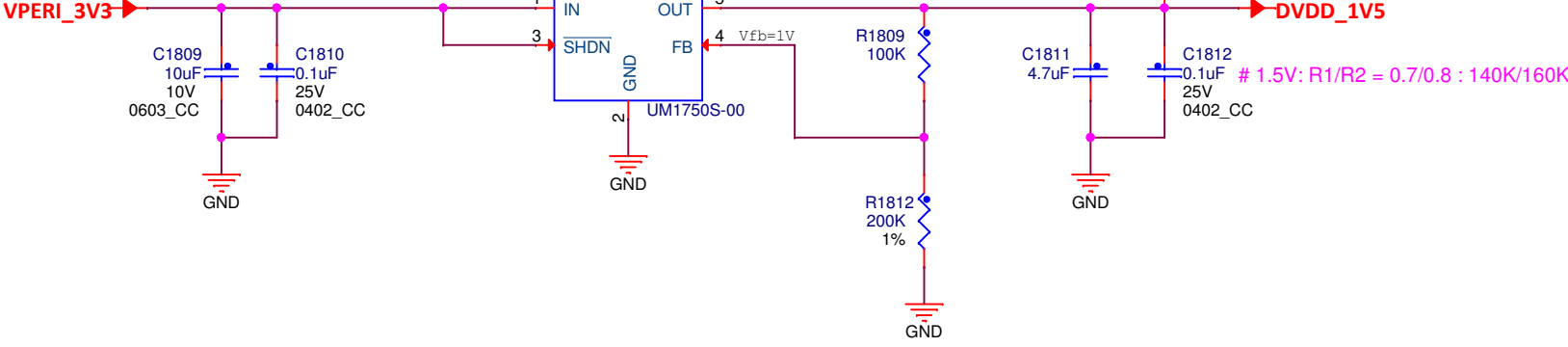
AVDD is 2.6-3.1V of sensor analog power (clean).
DOVDD is 1.7-3.1V of sensor digital IO power (clean). 1.8V is recommended.
DVDD is 1.5V of sensor core power (clean).



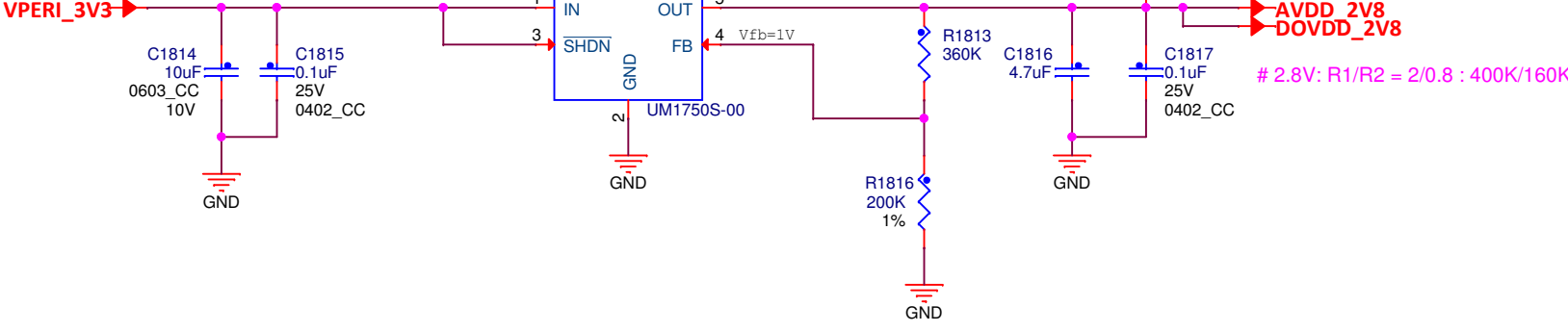
RSV for SIM



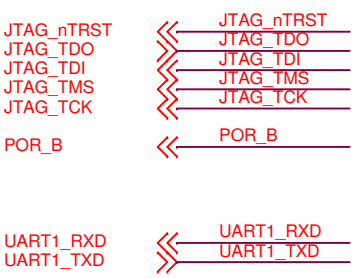
1.5V PWR



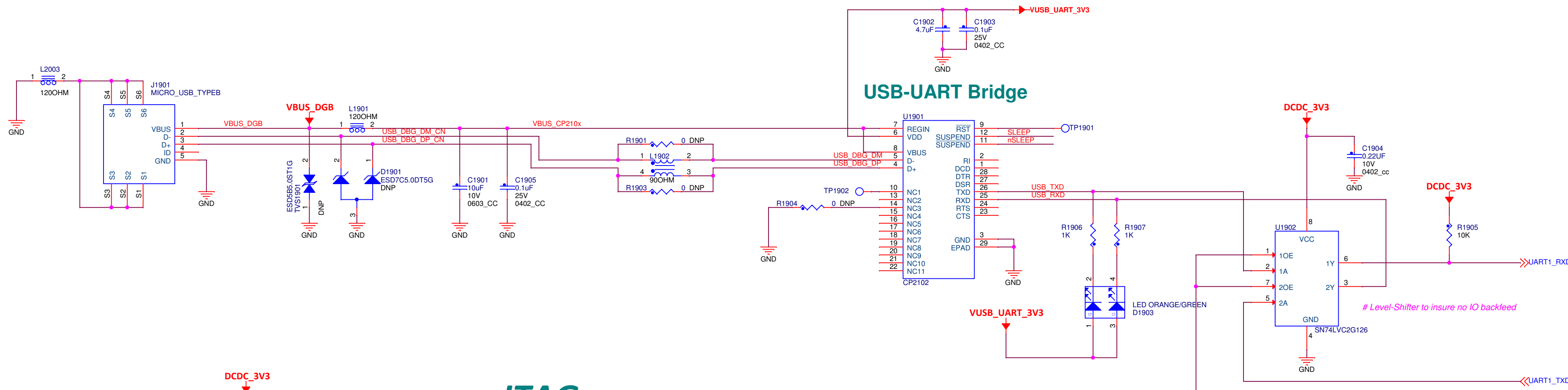
2.8V PWR



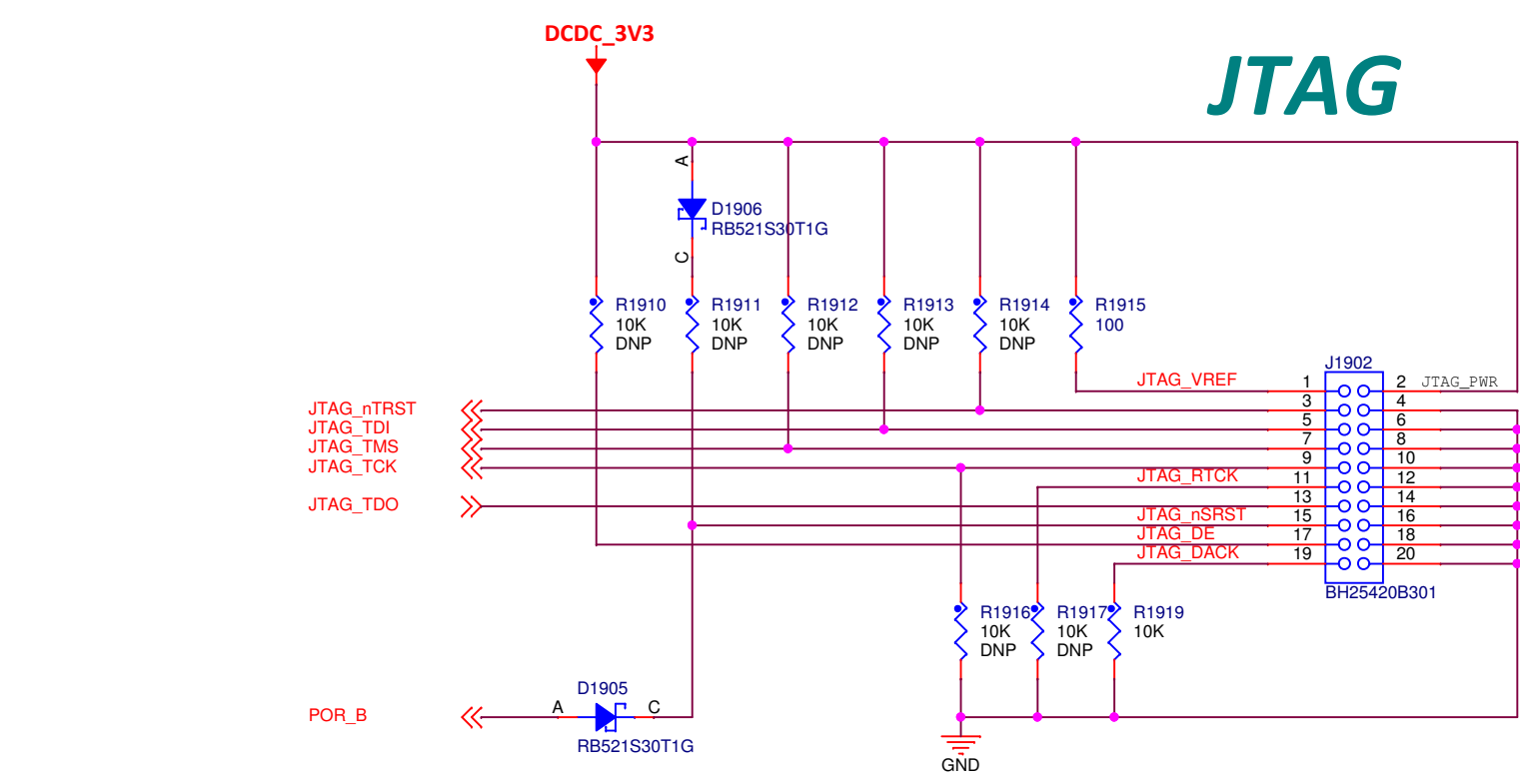
UART-USB DBG / JTAG



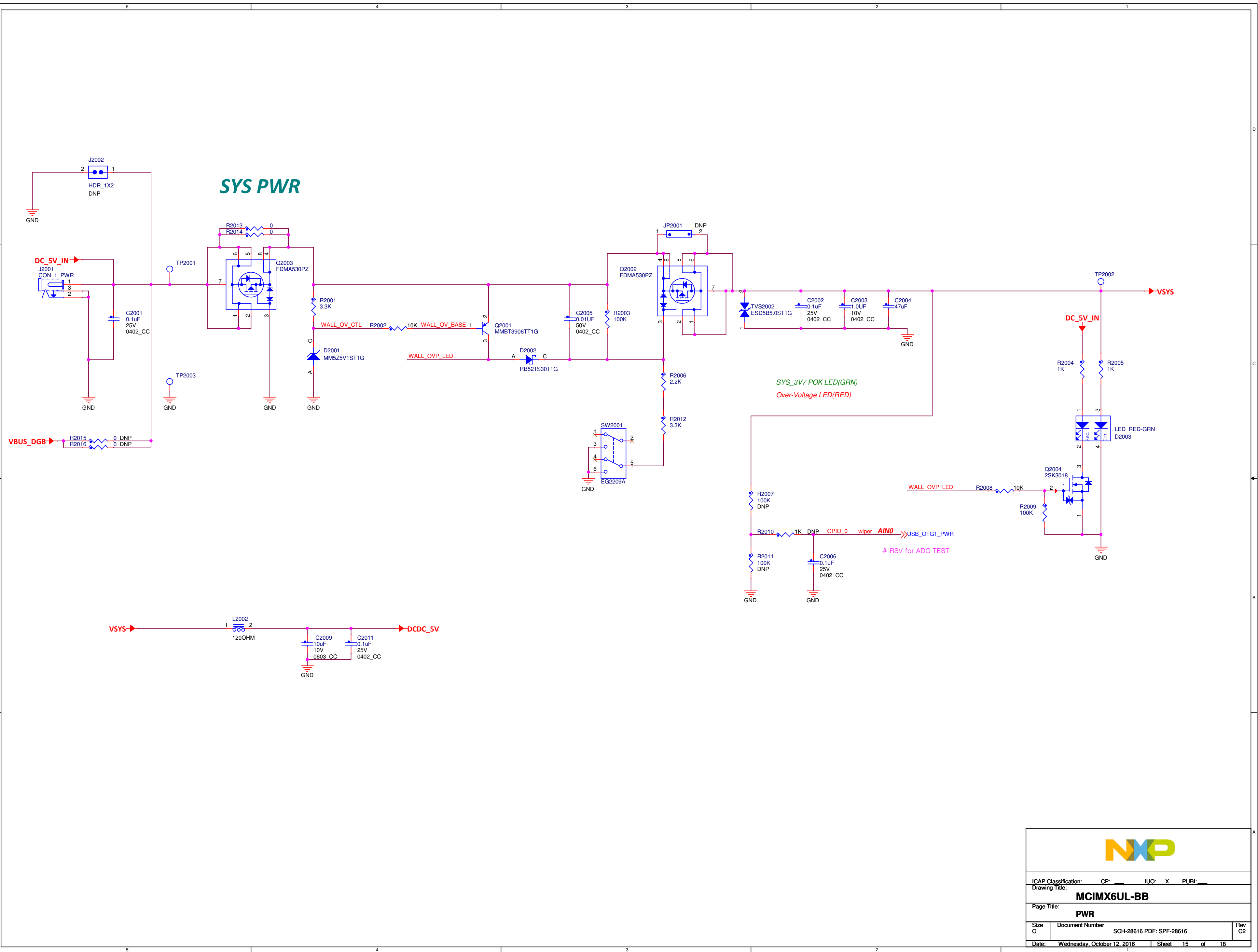
USB-UART Bridge



JTAG



ICAP Classification: CP: IVO: X PUBL:			
Drawing Title: MCIMX6UL-BB			
Page Title: DEBUG/JTAG			
Size C	Document Number SCH-28616 PDF: SPF-28616	Rev C2	
Date: Wednesday, October 19, 2016	Sheet 14	of 18	



CPU SODIMM TST/DBG

TP2101 DCDC_3V3

TP2102 UART1_TXD

TP2103 UART1_RXD

TP2104 GND

TP2105 GND

TP2106 USB_OTG1_DN

TP2107 USB_OTG1_DP

TP2108 GND

TP2109 GND

TP2110 USB_OTG1_VBUS

[illegible]

and as WDOG on CPL

ENET2_TXEN
ENET2_TXD1

ENET2_RXER
ENET2_TX_CLK

[illegible]

TP2120

JTAG_TDI

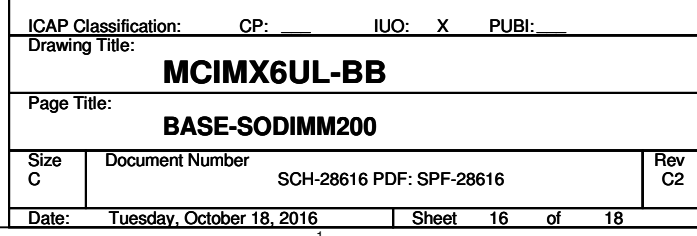
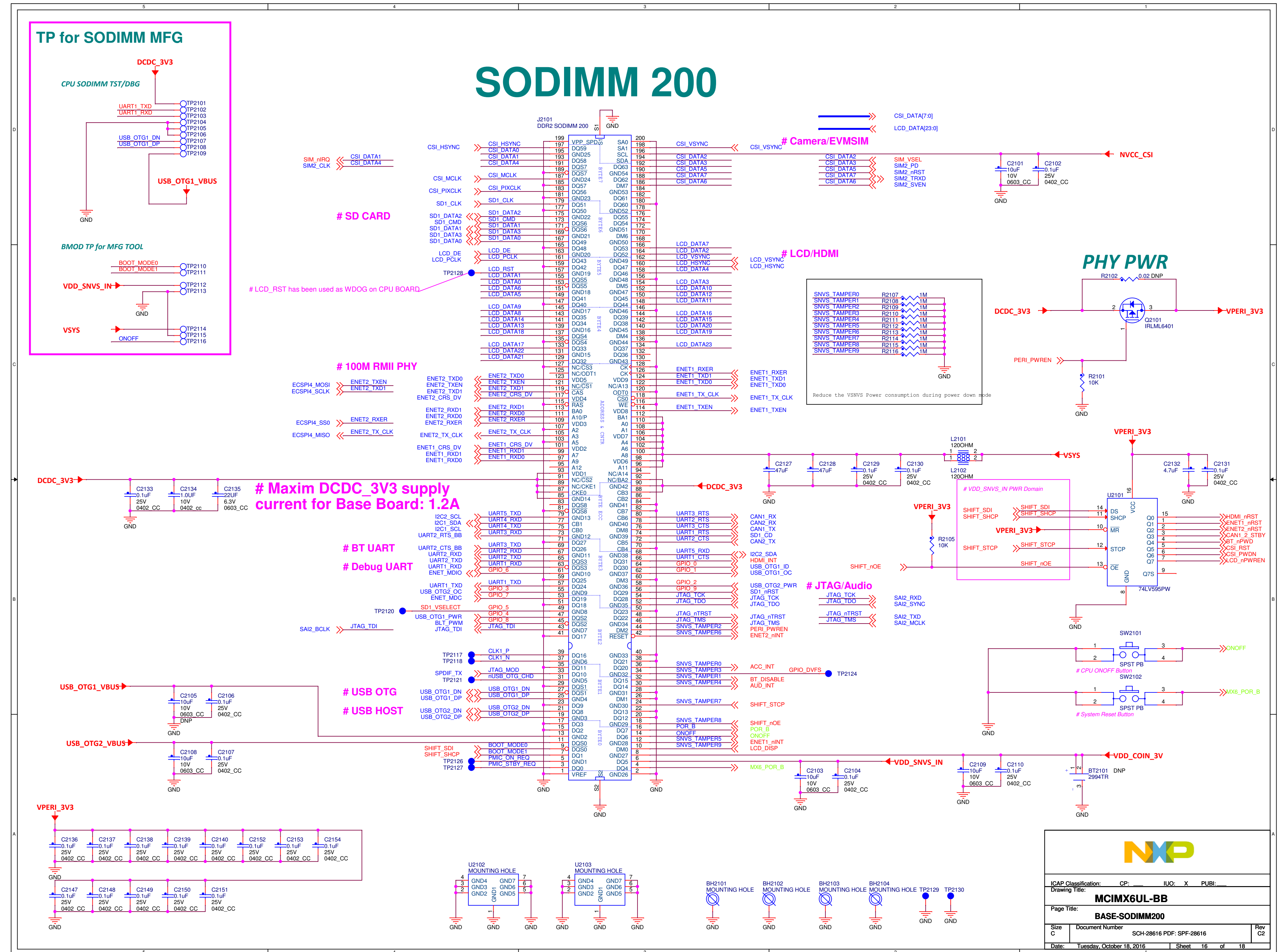
CSI_DATA2
CSI_DATA3
CSI_DATA5
CSI_DATA7
CSI_DATA6

SNVS_TA
SNVS_TA
SNVS_TA
SNVS_TA
SNVS_TA
SNVS_TA
SNVS_TA
SNVS_TA
SNVS_TA
SNVS_TA

The diagram shows a timing sequence for the VPERI_3V3 signal. It includes four signals: SHIFT_SDI, SHIFT_SHCP, SHIFT_STCP, and SHIFT_nOE. SHIFT_SDI and SHIFT_SHCP are shown as a single signal with a double arrow indicating a specific timing relationship. SHIFT_STCP is shown with a double arrow. SHIFT_nOE is shown as a signal that transitions from high to low. The signals are represented by horizontal lines with arrows indicating the direction of the signal transition.

JTAG_TCK
 JTAG_TDO
 JTAG_nTRST
 JTAG_TMS

IP2124



NOTE: EMV SIM will be placed on the daughter board

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done (this is boot option, we don't need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don't plan to change it.)	ALT7


All pins using ~src.en_system_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix. src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs_hp.snvs_sec_vio_in_5_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1'b0 in normal state, so harden is not triggerd in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon)



ICAP Classification:CP: IUO: X PUBI:

Drawing Title:MCIMX6UL-BB

Page Title:EMV SIM Daughter

Size C

Document NumberSCH-28616 PDF: SPF-28616

Rev C2

Date: Wednesday, October 12, 2016

Sheet 17 of 18

i.MX6UL IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	PAD DPU
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									100K PD
POR_B	src.POR_B	src.POR_B									100K PU
ONOFF	src.RESET_B	src.RESET_B									100K PU
SNVS_PMIC_ON_REQ	snvs_ip_wrapper.SNVS_WAKEUP_ALARM	snvs_ip_wrapper.PMIC_ON_REQ									100K PU
CCM_PMIC_STBY_REQ	cm.PMIC_STBY_REQ	cm.PMIC_STBY_REQ									100K PD
BOOT_MODE0	src.BOOT_MODE[0]	src.BOOT_MODE[0]									100K PD
BOOT_MODE1	src.BOOT_MODE[1]	src.BOOT_MODE[1]									100K PD
SNVS_TAMPER0	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[0]									100K PD
SNVS_TAMPER1	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[1]									100K PD
SNVS_TAMPER2	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[2]									100K PD
SNVS_TAMPER3	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[3]									100K PD
SNVS_TAMPER4	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[4]									100K PD
SNVS_TAMPER5	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[5]									100K PD
SNVS_TAMPER6	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[6]									100K PD
SNVS_TAMPER7	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[7]									100K PD
SNVS_TAMPER8	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[8]									100K PD
SNVS_TAMPER9	snvs_ip_wrapper.SNVS_TD1	snvs_ip_wrapper.TAMPER[9]									100K PD
JTAG_MOD	src.MOD	src.MOD									100K PU
JTAG_TMS	src.TMS	src.TMS									47K PU
JTAG_TDO	src.TDO	src.TDO									100K PU
JTAG_TDI	src.TDI	src.TDI									47K PU
JTAG_TCK	src.TCK	src.TCK									47K PU
JTAG_TRST_B	src.TRSTB	src.TRSTB									47K PU
GPIO1_I000	gpio1.i0[0]	gpio1.i0[0]									47K PU
GPIO1_I001	gpio1.i0[1]	gpio1.i0[1]									47K PU
GPIO1_I002	gpio1.i0[2]	gpio1.i0[2]									47K PU
GPIO1_I003	gpio1.i0[3]	gpio1.i0[3]									47K PU
GPIO1_I004	gpio1.i0[4]	gpio1.i0[4]									47K PU
GPIO1_I005	gpio1.i0[5]	gpio1.i0[5]									47K PU
GPIO1_I006	gpio1.i0[6]	gpio1.i0[6]									47K PU
GPIO1_I007	gpio1.i0[7]	gpio1.i0[7]									47K PU
GPIO1_I008	gpio1.i0[8]	gpio1.i0[8]									47K PU
GPIO1_I009	gpio1.i0[9]	gpio1.i0[9]									47K PU
UART1_TXD	gpio1.i0[16]	gpio1.i0[16]									47K PU
UART1_RXD	gpio1.i0[17]	gpio1.i0[17]									47K PU
UART1_CTS	gpio1.i0[18]	gpio1.i0[18]									47K PU
UART1_RTS	gpio1.i0[19]	gpio1.i0[19]									47K PU
UART2_TXD	gpio1.i0[20]	gpio1.i0[20]									47K PU
UART2_RXD	gpio1.i0[21]	gpio1.i0[21]									47K PU
UART2_CTS	gpio1.i0[22]	gpio1.i0[22]									47K PU
UART2_RTS	gpio1.i0[23]	gpio1.i0[23]									47K PU
UART3_TXD	gpio1.i0[24]	gpio1.i0[24]									47K PU
UART3_RXD	gpio1.i0[25]	gpio1.i0[25]									47K PU
UART3_CTS	gpio1.i0[26]	gpio1.i0[26]									47K PU
UART3_RTS	gpio1.i0[27]	gpio1.i0[27]									47K PU
UART4_TXD	gpio1.i0[28]	gpio1.i0[28]									47K PU
UART4_RXD	gpio1.i0[29]	gpio1.i0[29]									47K PU
UART5_TXD	gpio1.i0[30]	gpio1.i0[30]									47K PU
UART5_RXD	gpio1.i0[31]	gpio1.i0[31]									47K PU
ENET1_RXD0	enet1.rxd0	enet1.rxd0									47K PU
ENET1_TXD1	enet1.tx1	enet1.tx1									47K PU
ENET1_CRS_DV	enet1.crs_dv	enet1.crs_dv									47K PU
ENET1_TXD0	enet1.tx0	enet1.tx0									47K PU
ENET1_RXD1	enet1.rxd1	enet1.rxd1									47K PU
ENET1_TXEN	enet1.txen	enet1.txen									47K PU
ENET1_TXCLK	enet1.txclk	enet1.txclk									47K PU
ENET1_RXER	enet1.rxer	enet1.rxer									47K PU
ENET1_RXD0	enet1.rxd0	enet1.rxd0									47K PU
ENET2_RXD1	enet2.rxd1	enet2.rxd1									47K PU
ENET2_CRS_DV	enet2.crs_dv	enet2.crs_dv									47K PU
ENET2_TXD1	enet2.tx1	enet2.tx1									47K PU
ENET2_TXEN	enet2.txen	enet2.txen									47K PU
ENET2_TXCLK	enet2.txclk	enet2.txclk									47K PU
ENET3_RXER	enet3.rxer	enet3.rxer									47K PU
LCD_CLK	lcd.clk	lcd.clk									47K PU
LCD_ENABLE	lcd.enable	lcd.enable									47K PU
LCD_HSYNC	lcd.hsync	lcd.hsync									47K PU
LCD_VSYNC	lcd.vsync	lcd.vsync									47K PU
LCD_RESET	lcd.reset	lcd.reset									47K PU
LCD_DATA00	lcd.data00	lcd.data00									47K PU
LCD_DATA01	lcd.data01	lcd.data01									47K PU
LCD_DATA02	lcd.data02	lcd.data02									47K PU
LCD_DATA03	lcd.data03	lcd.data03									47K PU
LCD_DATA04	lcd.data04	lcd.data04									47K PU
LCD_DATA05	lcd.data05	lcd.data05									47K PU
LCD_DATA06	lcd.data06	lcd.data06									47K PU
LCD_DATA07	lcd.data07	lcd.data07									47K PU
LCD_DATA08	lcd.data08	lcd.data08									47K PU
LCD_DATA09	lcd.data09	lcd.data09									47K PU
LCD_DATA10	lcd.data10	lcd.data10									47K PU
LCD_DATA11	lcd.data11	lcd.data11									47K PU
LCD_DATA12	lcd.data12	lcd.data12									47K PU
LCD_DATA13	lcd.data13	lcd.data13									47K PU
LCD_DATA14	lcd.data14	lcd.data14									47K PU
LCD_DATA15	lcd.data15	lcd.data15									47K PU
LCD_DATA16	lcd.data16	lcd.data16									47K PU
LCD_DATA17	lcd.data17	lcd.data17									47K PU
LCD_DATA18	lcd.data18	lcd.data18									47K PU
LCD_DATA19	lcd.data19	lcd.data19									47K PU
LCD_DATA20	lcd.data20	lcd.data20									47K PU
LCD_DATA21	lcd.data21	lcd.data21									47K PU
LCD_DATA22	lcd.data22	lcd.data22									47K PU
LCD_DATA23	lcd.data23	lcd.data23									47K PU
NAND_RE_B	nand.re_b	nand.re_b									47K PU
NAND_WE_B	nand.we_b	nand.we_b									47K PU
NAND_DATA00	nand.data00	nand.data00									47K PU
NAND_DATA01	nand.data01	nand.data01									47K PU
NAND_DATA02	nand.data02	nand.data02									47K PU
NAND_DATA03	nand.data03	nand.data03									47K PU
NAND_DATA04	nand.data04	nand.data04									47K PU
NAND_DATA05	nand.data05	nand.data05									47K PU
NAND_DATA06	nand.data06	nand.data06									47K PU
NAND_DATA07	nand.data07	nand.data07									47K PU
NAND_ALE	nand.ale	nand.ale									47K PU
NAND_WP_B	nand.wp_b	nand.wp_b									47K PU
NAND_READY_B	nand.ready_b	nand.ready_b									47K PU
NAND_CE0_B	nand.ce0_b	nand.ce0_b									47K PU
NAND_CE1_B	nand.ce1_b	nand.ce1_b									47K PU
NAND_CLE	nand.cle	nand.cle									47K PU
NAND_DQS	nand.dqs	nand.dqs									47K PU
SD1_CMD	sd1.cmd	sd1.cmd									47K PU
SD1_CLK	sd1.clk	sd1.clk									47K PU
SD1_DATA0	sd1.data0	sd1.data0									47K PU
SD1_DATA1	sd1.data1	sd1.data1									47K PU
SD1_DATA2	sd1.data2	sd1.data2									47K PU
SD1_DATA3	sd1.data3	sd1.data3									47K PU
CSI_MCLK	csi.mclk	csi.mclk									47K PU
CSI_PIXCLK	csi.pixclk	csi.pixclk									47K PU
CSI_VSYNC	csi.vsync	csi.vsync									47K PU
CSI_HSYNC	csi.hsync	csi.hsync									47K PU
CSI_DATA00	csi.data00	csi.data00									47K PU
CSI_DATA01	csi.data01	csi.data01									47K PU
CSI_DATA02	csi.data02	csi.data02									47K PU
CSI_DATA03	csi.data03	csi.data03									47K PU
CSI_DATA04	csi.data04	csi.data04									47K PU
CSI_DATA05	csi.data05	csi.data05									47K PU
CSI_DATA06	csi.data06	csi.data06									47K PU
CSI_DATA07	csi.data07	csi.data07									47K PU
gpio5.i0[10]	gpio5.i0[10]	gpio5.i0[10]									47K PU
gpio5.i0[11]	gpio5.i0[11]	gpio5.i0[11]									47K PU
gpio5.i0[12]	gpio5.i0[12]	gpio5.i0[12]									47K PU
gpio5.i0[13]	gpio5.i0[13]	gpio5.i0[13]									47K PU
gpio5.i0[14]	gpio5.i0[14]	gpio5.i0[14]									47K PU
gpio5.i0[15]	gpio5.i0[15]	gpio5.i0[15]									47K PU
gpio5.i0[16]	gpio5.i0[16]	gpio5.i0[16]									47K PU
gpio5.i0[17]	gpio5.i0[17]	gpio5.i0[17]									47K PU
gpio5.i0[18]	gpio5.i0[18]	gpio5.i0[18]									47K PU
gpio5.i0[19]	gpio5.i0[19]	gpio5.i0[19]									47K PU
gpio5.i0[20]	gpio5.i0[20]	gpio5.i0[20]									47K PU
gpio5.i0[21]	gpio5.i0[21]	gpio5.i0[21]									47K PU
gpio5.i0[22]	gpio5.i0[22]	gpio5.i0[22]									47K PU
gpio5.i0[23]	gpio5.i0[23]	gpio5.i0[23]									47K PU
gpio5.i0[24]	gpio5.i0[24]	gpio5.i0[24]									47K PU
gpio5.i0[25]	gpio5.i0[25]	gpio5.i0[25]									47K PU
gpio5.i0[26]	gpio5.i0[26]	gpio5.i0[26]									47K PU
gpio5.i0[27]	gpio5.i0[27]	gpio5.i0[27]									47K PU
gpio5.i0[28]	gpio5.i0[28]	gpio5.i0[28]									47K PU
gpio5.i0[29]	gpio5.i0[29]	gpio5.i0[29]									47K PU
gpio5.i0[30]	gpio5.i0[30]	gpio5.i0[30]									47K PU
gpio5.i0[31]	gpio5.i0[31]	gpio5.i0[31]									47K PU
sdma.ext_event[0]	sdma.ext_event[0]	sdma.ext_event[0]									47K PU
sdma.ext_event[1]	sdma.ext_event[1]	sdma.ext_event[1]									47K PU
mqsr RIGHT	mqsr RIGHT	mqsr RIGHT									47K PU
mqsr LEFT	mqsr LEFT	mqsr LEFT									47K PU
osc32k_32K_OUT	osc32k_32K_OUT	osc32k_32K_OUT									47K PU
anatop_24M_OUT	anatop_24M_OUT	anatop_24M_OUT									47K PU
enet1.1588_EVENT0_IN	enet1.1588_EVENT0_IN	enet1.1588_EVENT0_IN									47K PU
enet1.1588_EVENT0_OUT	enet1.1588_EVENT0_OUT	enet1.1588_EVENT0_OUT									47K PU
src.ANY_PU_RESET	src.ANY_PU_RESET	src.ANY_PU_RESET									47K PU
src.TESTER_ACK	src.TESTER_ACK	src.TESTER_ACK									47K PU
cm.PLL2_BYP	cm.PLL2_BYP	cm.PLL2_BYP									47K PU
cm.PLL3_BYP	cm.PLL3_BYP	cm.PLL3_BYP									47K PU